

## 800mA Dual-rail Very Low Dropout LDO

### General Description

The ET557ADJY1B is a CMOS-based low-dropout, low-power linear regulators, offering 800mA with NMOS pass transistor and a separate bias supply voltage (VBIAS). The device provides very stable, accurate output voltage with low noise, high ripple rejection and low supply current suitable for space constrained, noise sensitive application. The ET557ADJY1B series consist of an accurate voltage-reference block, an error amplifier, a thermal-shutdown circuit, and a current limit circuit.

The ET557ADJY1B is available in the DFN6(1.2mm ×1.2mm) package.

### Features

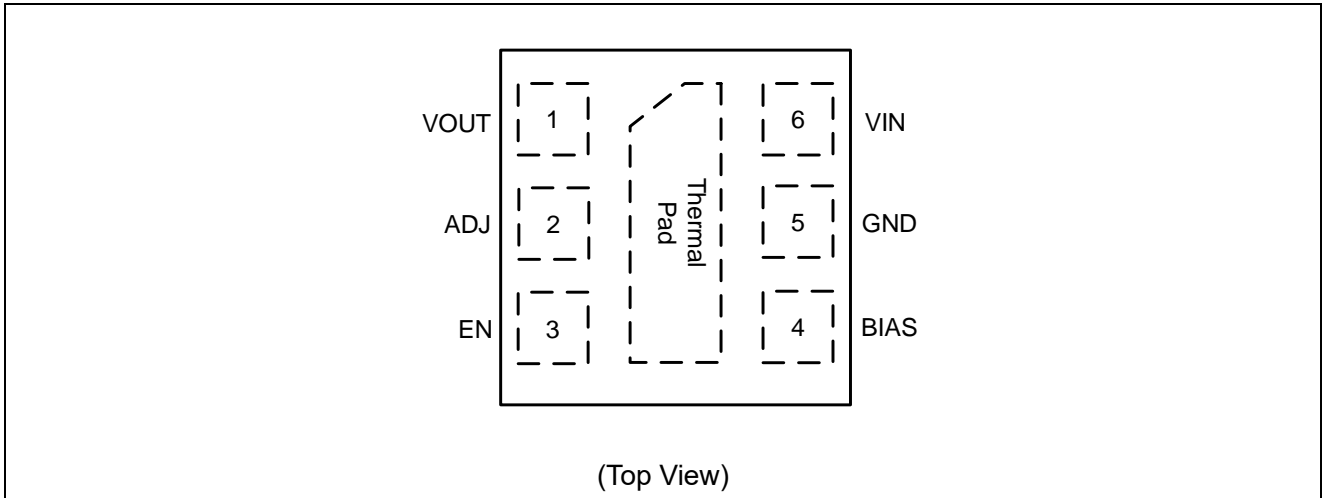
- Wide  $V_{IN}$  Input Voltage Range: 0.8V to 5.5V
- Wide  $V_{BIAS}$  Voltage Range: 2.7V to 5.5V
- ADJ Output Voltage Range: 0.8V to 3.6V
- Very Low  $V_{BIAS}$  Input Current of Typ. 80 $\mu$ A
- Ultra Low Dropout: Typ. 220mV at 800mA, 1.2V Output, 2.8V Bias
- Built-in Over Current Protection and Thermal Shutdown Circuit
- Built-in Auto-discharging Circuit
- Built-in Under Voltage Lock-out
- Stable with a 2.2 $\mu$ F Ceramic Capacitor
- Package: DFN6 (1.2mm × 1.2mm)
- MSL: Level 1

### Applications

- Constant-Voltage Power Supply for Battery-Powered Device
- Constant-Voltage Power Supply for Smartphones, Tablets
- Constant-Voltage Power Supply for Cameras, DVRs, STB and Camcorders

# ET557ADJY1B

## Pin Configuration

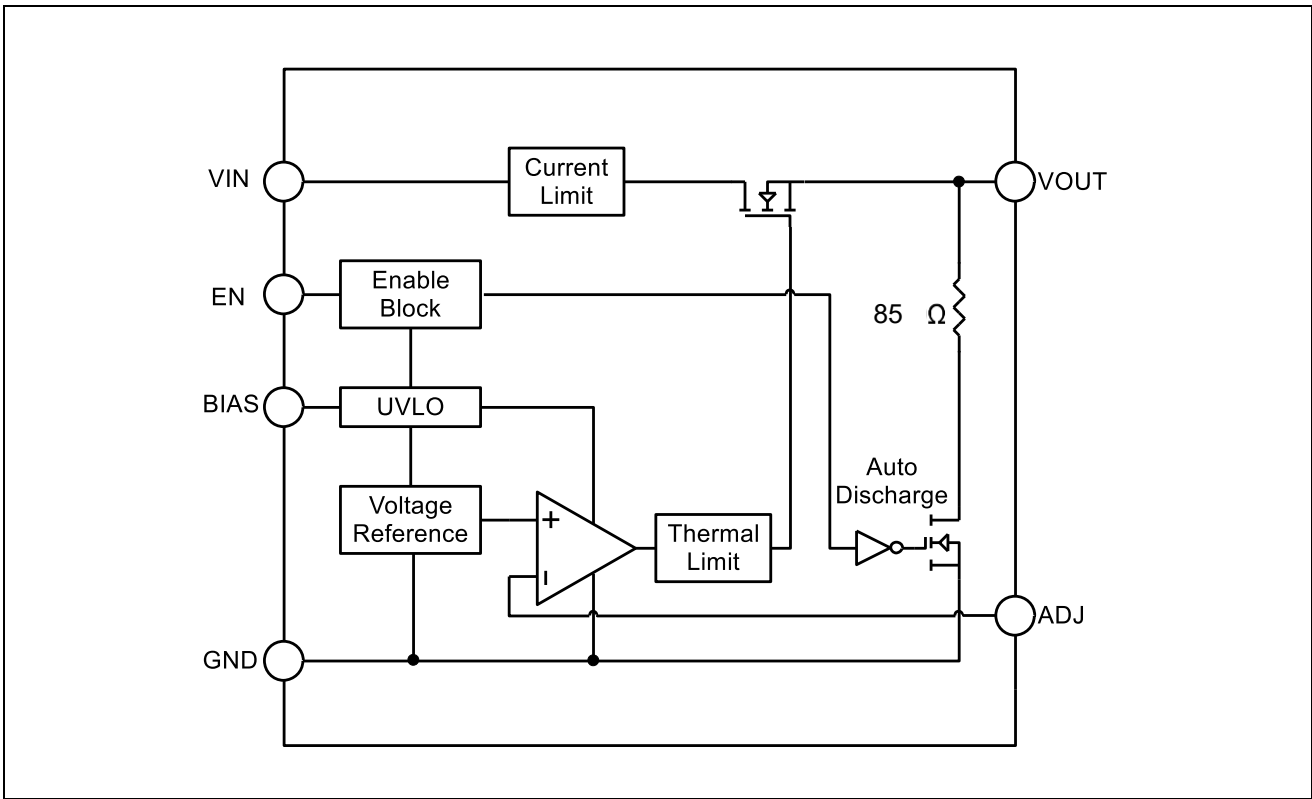


## Pin Function

Symbol	Pin Name	Pin Description
VOUT	1	The power output of the device.
ADJ	2	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
EN	3	Enable Input.
BIAS	4	Input voltage for controlling circuit.
GND	5	Ground pin.
VIN	6	Input voltage Pin. Large bulk capacitance should be placed closely to this pin. A 1 $\mu$ F ceramic capacitor is recommended at this pin.
TP		Thermal pad, connect to GND

# ET557ADJY1B

## Block Diagram



## Functional Description

The ET557ADJY1B dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from  $V_{IN}$  voltage. All the low current internal control circuitry is powered from the  $V_{BIAS}$  voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability.  $V_{IN}$  to  $V_{OUT}$  operating voltage difference can be very low compared with standard PMOS regulators in very low  $V_{IN}$  applications.

The ET557ADJY1B offers smooth monotonic start-up.

## Input and output Capacitor

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from  $2.2\mu\text{F}$  to  $4.7\mu\text{F}$ . The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. In applications where no low input supplies impedance available (PCB inductance in  $V_{IN}$  and/or  $V_{BIAS}$  inputs as example), the recommended  $C_{IN} = 1\mu\text{F}$  and  $C_{BIAS} = 0.1\mu\text{F}$  or greater.

## Enable Pin Operation

The ET557ADJY1B is turned on by setting the EN pin to "H". The threshold limits are covered in the electrical characteristics table in this datasheet. When the EN pin is not used, connect the EN pin with  $V_{BIAS}$  to keep the LDO in operating mode.

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## Current Limit Protection

When output current of V<sub>OUT</sub> pin is higher than current limit threshold or the V<sub>OUT</sub> pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage.

## Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool down. When the junction temperature reduces to approximately +145°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

## Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of V<sub>OUT</sub> in very short time. The Auto-Discharging function is optional.

## Output Voltage Adjust

The required output voltage of Adjustable devices can be adjusted from V<sub>REF</sub> to 3.6 V using two external resistors. Typical application schematics is shown blow.

$$V_{OUT} = V_{REF} \times (1+R1/R2)$$

Typical value of V<sub>REF</sub> is 0.8V. It is recommended to keep the total serial resistance of resistors (R1+R2) not greater than 100KΩ.

The output voltage needs to take into account the error caused by the resistance accuracy.

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## Absolute Maximum Ratings

Symbol	Item	Rating	Unit
V <sub>IN</sub>	Input Voltage(VIN Pin)	-0.3 to 6.0	V
V <sub>BIAS</sub>	Input Voltage (VBIAS Pin)	-0.3 to 6.0	V
V <sub>EN</sub>	Input Voltage (EN Pin)	-0.3 to 6.0	V
V <sub>BIAS</sub>	Input Voltage (ADJ Pin)	-0.3 to 6.0	V
V <sub>OUT</sub>	Output Voltage	-0.3 to 6.0	V
I <sub>OUT_MAX</sub>	Maximum Load Current	800	mA
PD <sub>MAX</sub>	Maximum Power Consumption	640	mW
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>J</sub>	Operating Junction Temperature	-40 to +150	°C
V <sub>ESD</sub>	Human Body Model (JESD22-A114)	±3000	V
	Charged Device Model (JESD22-C101)	±1500	V
I <sub>LU</sub>	Latch up Current Maximum Rating (JESD78E)	±200	mA

## Recommended Operating Conditions

Symbol	Item	Rating	Unit
V <sub>IN</sub>	IN Input Voltage	V <sub>OUT</sub> + V <sub>DROP</sub> to 5.5	V
V <sub>BIAS</sub>	BIAS Input Voltage	2.7 to 5.5 & V <sub>BIAS</sub> ≥V <sub>OUT</sub> +1.4V	V
I <sub>OUT</sub>	Output Current	0 to 800	mA
T <sub>A</sub>	Operating Ambient Temperature	-40 to +85	°C
C <sub>IN</sub>	Effective Input Ceramic Capacitor Value	0.47 to 10	μF
C <sub>BIAS</sub>	Effective Input Ceramic Capacitor Value	0.047 to 4.7	μF
C <sub>OUT</sub> <sup>(1)</sup>	Effective Output Ceramic Capacitor Value	1 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

**Notes 1:** When V<sub>OUT</sub> < 1.0V, C<sub>OUT</sub> should larger than 2.2μF.

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## Electrical Characteristics

(Unless otherwise noted,  $V_{IN} = V_{OUT} + 0.3V$ ,  $V_{BIAS} = 2.7V$  or  $V_{OUT} + 1.6V$  whichever is greater,  $I_{OUT} = 1mA$ ,  $C_{IN} = 1\mu F$ ,  $C_{OUT} = 2.2\mu F$ ,  $C_{BIAS} = 0.1\mu F$ ,  $T_A = -40^\circ C \sim 85^\circ C$ . Typical values are at  $T_A = 25^\circ C$ )

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IN}^{(2)}$	Input Voltage Range	$V_{IN} > V_{OUT}$	$V_{OUT} + V_{DROP}$		5.5	V
$V_{BIAS}$	$V_{BIAS}$ Voltage Range	$V_{BIAS} > V_{OUT} + 1.4V$	2.7		5.5	V
$V_{UVLO}$	Under-Voltage	$V_{BIAS}$ Rising	1.8	2.1	2.5	V
$V_{UVLO\_HYS}$	Lock-Out	Hysteresis	0.10	0.25	0.40	
$I_{ON\_BIAS}^{(3)}$	$V_{BIAS}$ Current	Active mode: $V_{EN} = V_{BIAS}$	55	80	110	$\mu A$
$I_{OFF\_BIAS}$		$V_{EN} = 0V$		0.15	1	$\mu A$
$V_{OUT}$	$V_{OUT}$ Voltage	$I_{OUT} = 1mA \sim 0.8A$ , $T_A = 25^\circ C$ , OUT connected to ADJ	784		816	mV
		$I_{OUT} = 1mA \sim 0.5A$ , $T_A = -40^\circ C \sim 85^\circ C$ , OUT connected to ADJ	784		816	mV
		$I_{OUT} = 1mA \sim 0.8A$ , $T_A = -40^\circ C \sim 85^\circ C$ , OUT connected to ADJ	780		820	mV
$V_{DROP}^{(4)}$	Dropout Voltage	$I_{OUT} = 0.5A$ , $V_{OUT} = 1.2V$ , $V_{BIAS} = 2.8V$		125	230	mV
		$I_{OUT} = 0.8A$ , $V_{OUT} = 1.2V$ , $V_{BIAS} = 2.8V$		220	350	
		$I_{OUT} = 0.5A$ , $V_{OUT} = 1.8V$ , $V_{BIAS} = 3.2V$		145	250	
$I_{LIM}$	Limit Current		800	1450	1800	mA
$I_{SC}$	Short Current		30	130	280	mA
$Reg_{LOAD}$	Load Regulation	$V_{BIAS} = 2.7V$ or $V_{OUT} + 1.6V$ , whichever is greater, $1mA \leq I_{OUT} \leq 800mA$		2	20	mV
$Reg_{LINE}$	$V_{IN}$ Line Regulation	$V_{OUT} + 0.3V \leq V_{IN} \leq 5V$ ( $V_{BIAS} = V_{OUT} + 1.6V$ , $I_{OUT} = 1mA$ )		0.01	0.1	%/V
	$V_{BIAS}$ Line Regulation	2.7V or $V_{OUT} + 1.4V$ , whichever is greater < $V_{BIAS} < 5.5V$ ( $V_{IN} = V_{OUT} + 0.3V$ , $I_{OUT} = 1mA$ )		0.01	0.1	%/V
$PSRR^{(5)}$	Ripple Rejection	$V_{BIAS} = 2.7V$ or $V_{OUT} + 1.6V$ , whichever is greater, $V_{IN}$ to $V_{OUT}$ , $f = 1kHz$ , Ripple 0.2Vp-p, $V_{IN} = V_{OUT} + 0.5V$ , $I_{OUT} = 30mA$	65	80		dB
		$V_{BIAS} = 2.7V$ or $V_{OUT} + 1.6V$ , whichever is greater, $V_{BIAS}$ to $V_{OUT}$ , $f = 1kHz$ , Ripple 0.2Vp-p, $V_{IN} = V_{OUT} + 0.5V$ , $I_{OUT} = 30mA$	65	80		
$e_N^{(5)}$	Output Noise	$V_{IN} = V_{OUT} + 0.5V$ , $f = 10Hz$ to $100kHz$	$30 \times V_{OUT}$	$45 \times V_{OUT}$	$65 \times V_{OUT}$	$\mu V_{RMS}$

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## Electrical Characteristics(Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I <sub>EN</sub>	EN Pull-down Current	V <sub>EN</sub> =5.5V, V <sub>BIAS</sub> =5.5V		0.2	1	μA
V <sub>IH</sub>	EN Input Voltage High		0.9		5.5	V
V <sub>IL</sub>	EN Input Voltage Low		0.0		0.4	V
R <sub>DIS</sub>	Output Resistance of Auto Discharge at Off State	V <sub>BIAS</sub> =3.8V, V <sub>IN</sub> =5.5V, V <sub>EN</sub> =0V, I <sub>OUT</sub> =10mA	40	85	150	Ω
V <sub>TRLN</sub> <sup>(5)</sup>	Line Transient	V <sub>IN</sub> = V <sub>OUT</sub> +0.3V to 5.5V in 10us, V <sub>BIAS</sub> = V <sub>OUT</sub> +1.6V, V <sub>OUT</sub> =1.2V, I <sub>OUT</sub> =1mA, T <sub>A</sub> =25°C		5	30	mV
		V <sub>IN</sub> =5.5V to V <sub>OUT</sub> +0.3V in 10us, V <sub>BIAS</sub> = V <sub>OUT</sub> +1.6V, V <sub>OUT</sub> =1.2V, I <sub>OUT</sub> =1mA, T <sub>A</sub> =25°C		5	30	mV
V <sub>TRLD</sub> <sup>(5)</sup>	Load Transient	I <sub>OUT</sub> =1mA to 500mA in 10us V <sub>OUT</sub> =1.2V, V <sub>IN</sub> = V <sub>OUT</sub> +0.5V, V <sub>BIAS</sub> = 2.7V or V <sub>OUT</sub> +1.6V, whichever is greater, T <sub>A</sub> =25°C		110	150	mV
		I <sub>OUT</sub> =500mA to 1mA in 10us V <sub>OUT</sub> =1.2V, V <sub>IN</sub> = V <sub>OUT</sub> +0.5V, V <sub>BIAS</sub> = 2.7V or V <sub>OUT</sub> +1.6V, whichever is greater, T <sub>A</sub> =25°C		85	120	mV
t <sub>ON</sub>	Turn-On Time	From Assertion of V <sub>EN</sub> to V <sub>OUT</sub> =98%V <sub>OUT(NOM)</sub>	60	150	300	μs
T <sub>SD</sub> <sup>(5)</sup>	Thermal Shutdown Temperature	Temperature increasing	145	160	175	°C
T <sub>SR</sub> <sup>(5)</sup>	Thermal Shutdown Released Temperature	Temperature decreasing	120	135	150	°C

**Notes 2:** The maximum input voltage should take into account the maximum power consumption (P<sub>D(MAX)</sub>).

The calculation formula is as follows:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}$$

The maximum power consumption of the circuit is 640mW.

$$V_{IN(MAX)} = 640mW / I_{OUT} + V_{OUT}$$

For example:

If V<sub>OUT</sub>= 1.2V, I<sub>OUT</sub>=800mA, the maximum input voltage is V<sub>IN(MAX)</sub>=640mW / 800mA+1.2=2.0V

If I<sub>OUT</sub> >500mA, V<sub>BIAS</sub> should be bigger than V<sub>OUT</sub>+1.6V.

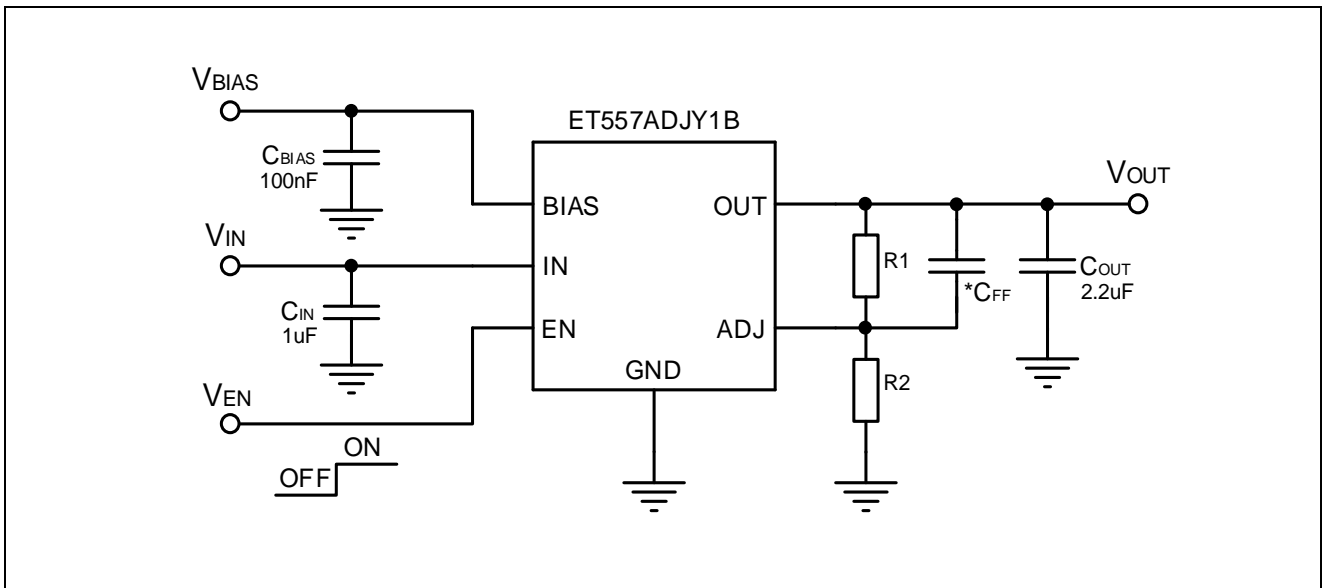
**Notes 3:** Since the power on process of BIAS needs a large current, the BIAS input voltage should have a current driving capacity of more than 10mA.

**Notes 4:** V<sub>DROP</sub> FT test method: test the V<sub>OUT</sub> voltage at V<sub>SET</sub> +V<sub>DROPMAX</sub> with output current.

**Notes 5:** Guaranteed by design and characterization. not a FT item.

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## Application Circuits



**Notes 6:** Adjust Version:  $V_{OUT} = 0.8 \times (1 + R1/R2)$ ,  $(R1 + R2)$  no greater than 100k $\Omega$ .

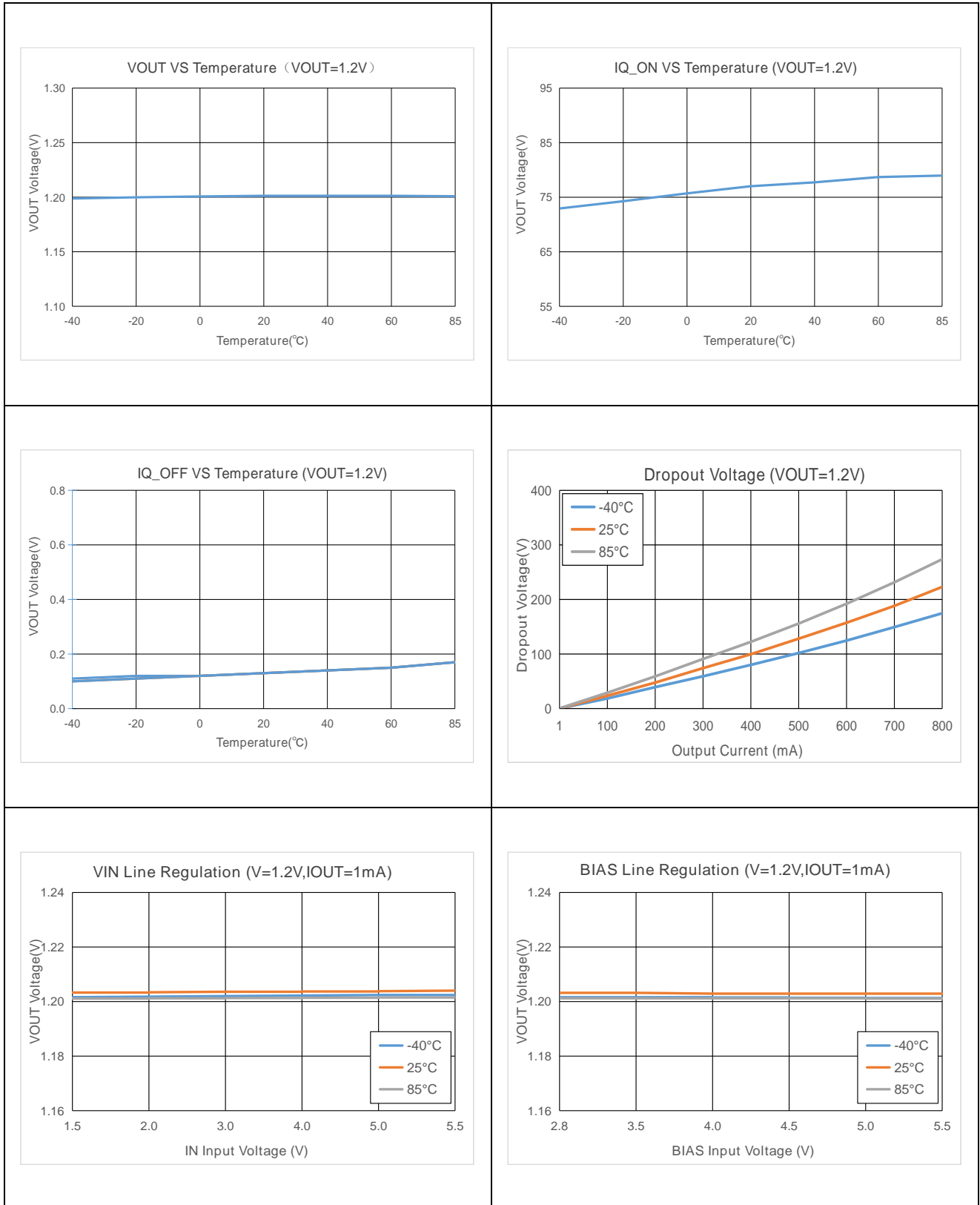
**Notes 7:** The feedforward capacitor  $C_{FF}$  is optional for the optimization of transient response.



# ET557ADJY1B

## Typical Characteristics

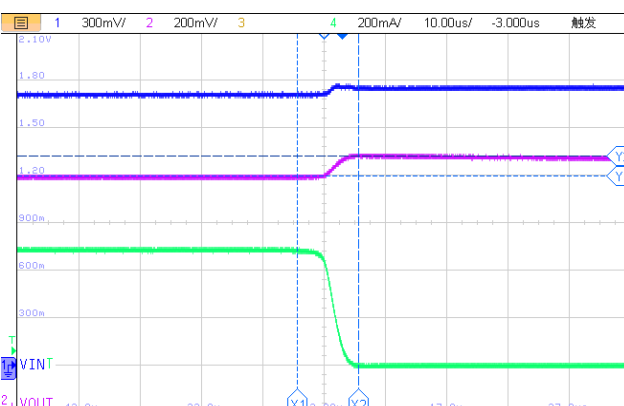
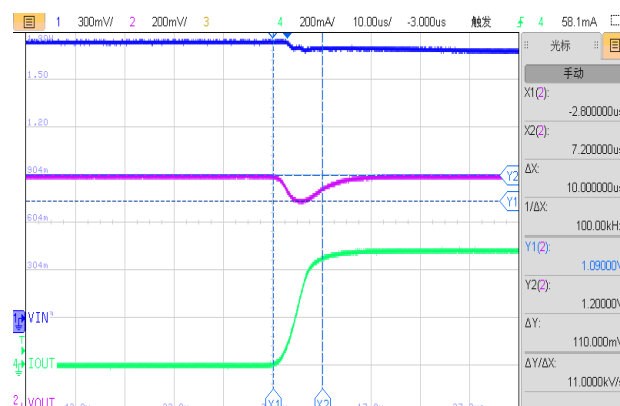
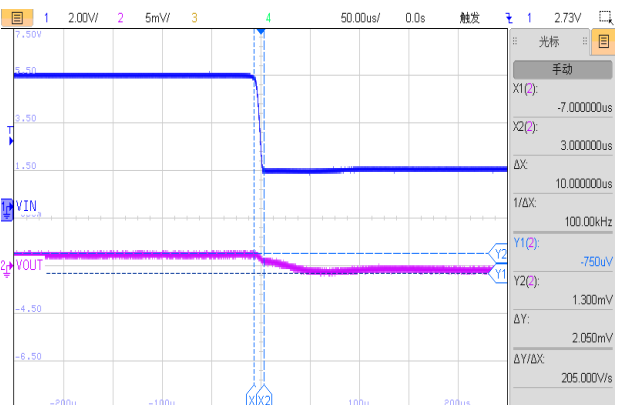
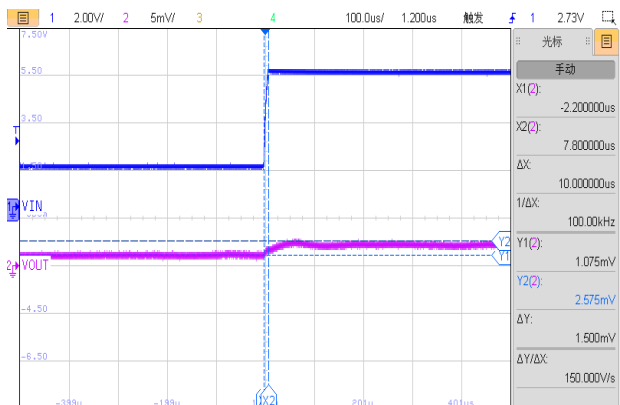
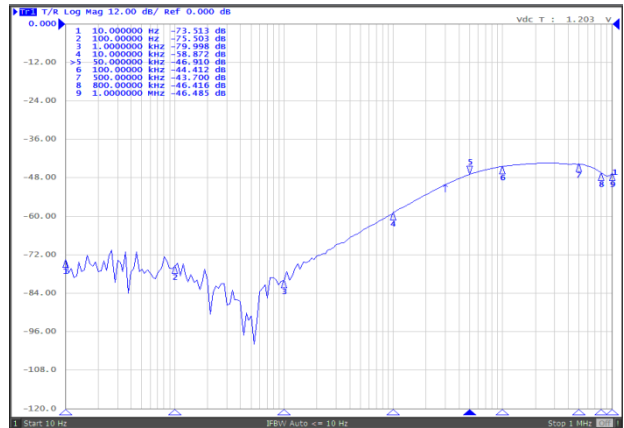
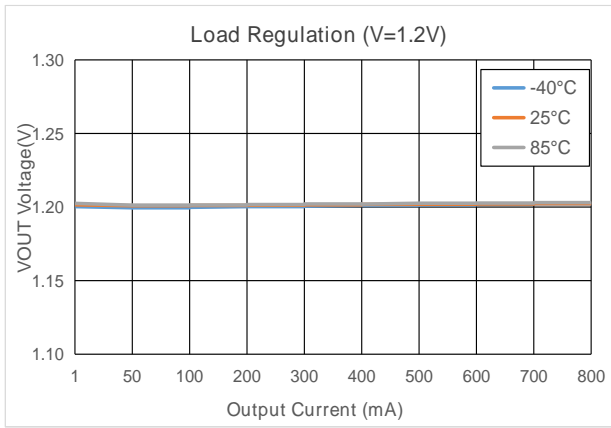
( $V_{OUT}=1.2V$ ,  $V_{IN}=V_{OUT}+0.3V$ ,  $V_{BIAS}=V_{OUT}+1.6V$ ,  $C_{IN}=1\mu F$ ,  $C_{OUT}=2.2\mu F$ ,  $C_{BIAS}=1\mu F$ ,  $T_A=-40^{\circ}C\sim+85^{\circ}C$ )



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## Typical Characteristics(Continued)

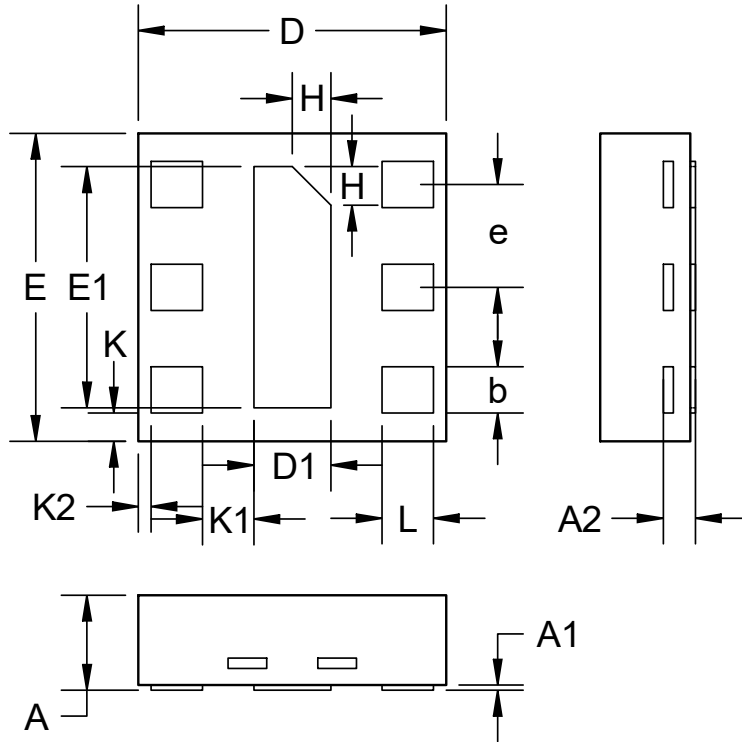
( $V_{OUT}=1.20V$ ,  $V_{IN}=V_{OUT}+0.3V$ ,  $V_{BIAS}=V_{OUT}+1.6V$ ,  $C_{IN}=1\mu F$ ,  $C_{OUT}=2.2\mu F$ ,  $C_{BIAS}=1\mu F$ ,  $T_A=-40^{\circ}C\sim+85^{\circ}C$ )



# ET557ADJY1B

## Package Dimension

DFN6(1)

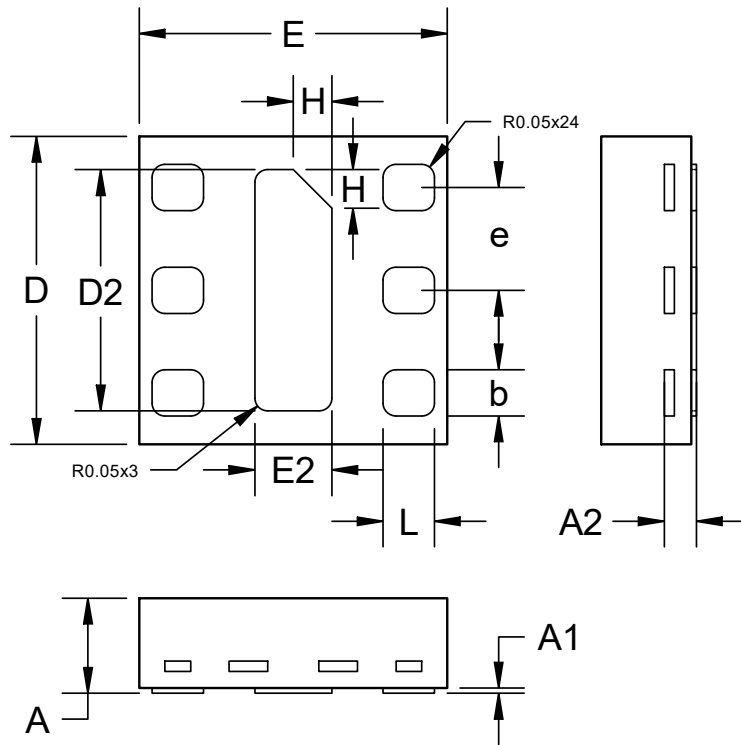


COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.34	0.37	0.42
A1	0.00	0.02	0.05
A2	0.10REF		
b	0.13	0.18	0.23
D	1.10	1.20	1.30
E	1.10	1.20	1.30
D1	0.25	0.30	0.35
E1	0.89	0.94	0.99
e	0.30	0.40	0.50
H	0.15REF		
K	0.11REF		
K1	0.15	0.20	0.25
K2	0.05REF		
L	0.15	0.20	0.25

# ET557ADJY1B

DFN6(2)

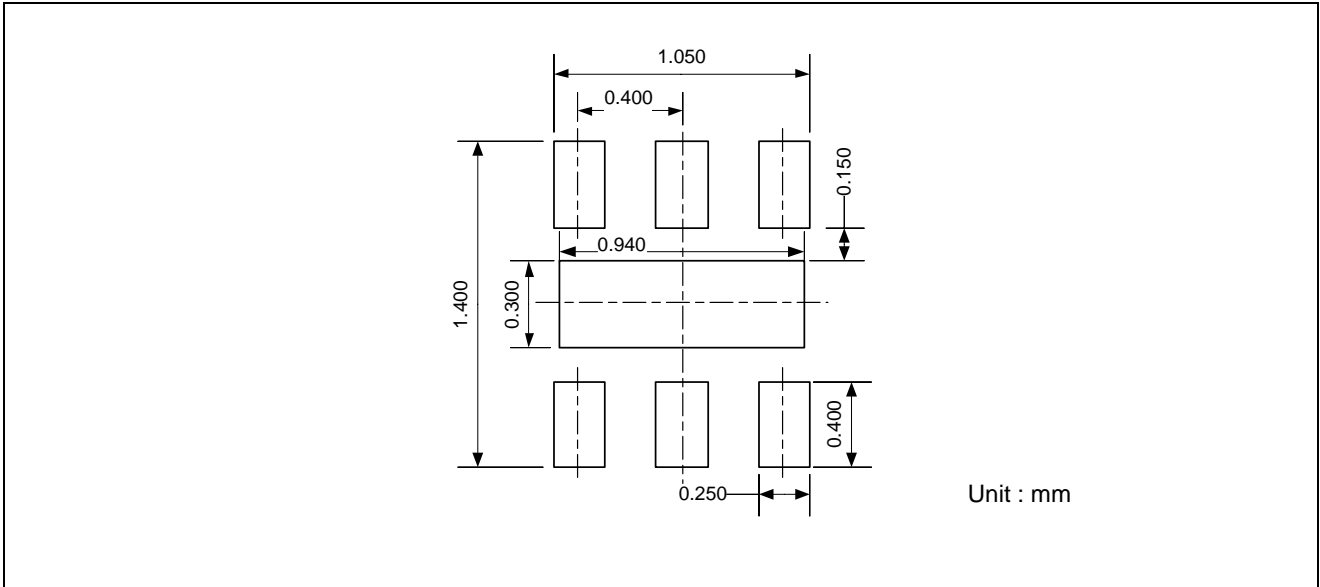


COMMON DIMENSIONS  
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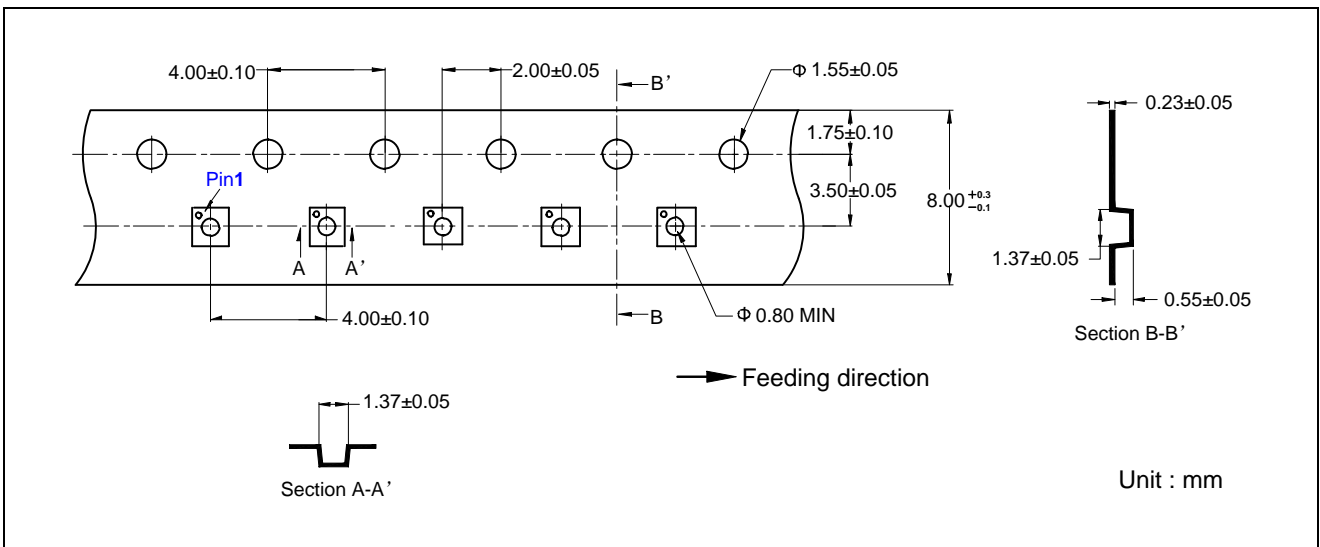
SYMBOL	MIN	NOM	MAX
A	0.30	0.35	0.42
A1	0.00	0.02	0.05
A2	0.125REF		
D	1.15	1.20	1.25
E	1.15	1.20	1.25
b	0.13	0.18	0.23
L	0.15	0.20	0.25
D2	0.89	0.94	0.99
E2	0.25	0.30	0.35
e	0.40 BSC		
H	0.15 REF		

# ET557ADJY1B

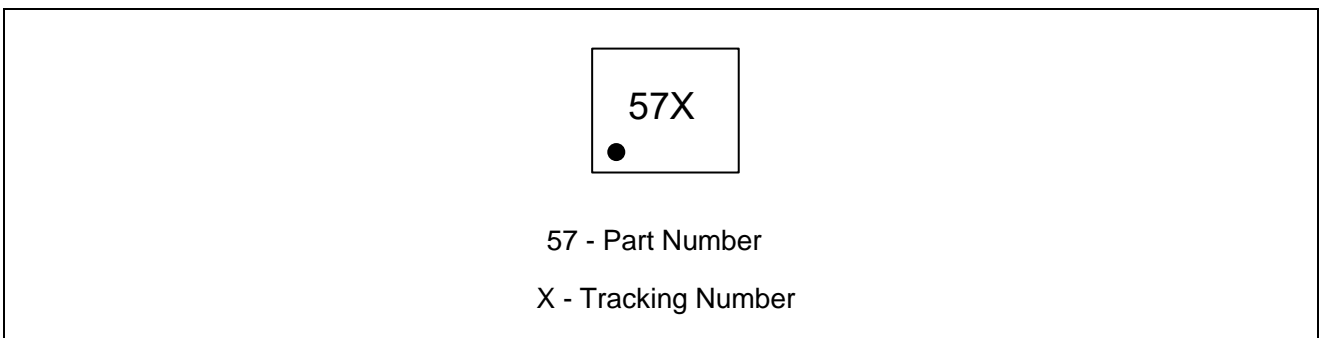
## Recommend PCB Layout



## Reel



## Marking Information



# ET557ADJY1B

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## Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-08-22	Initial Version	Yangxx	Liuyg	Liujy
0.1	2023-11-02	Add New Package Information	Tugz	Liuyg	Liujy
0.2	2023-11-15	Update Package Information	Tugz	Liuyg	Liujy
0.3	2024-05-30	Update SPEC	Tugz	Liuyg	Liujy
1.0	2024-08-07	Official Version,Update SPEC	Tugz	Liuyg	Liujy
1.1	2024-11-15	Update Package Dimension	Tugz	Liuyg	Liujy