

8-Bit Shift Registers with Output Latches

General Description

The 74HC595 is a high speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

Features

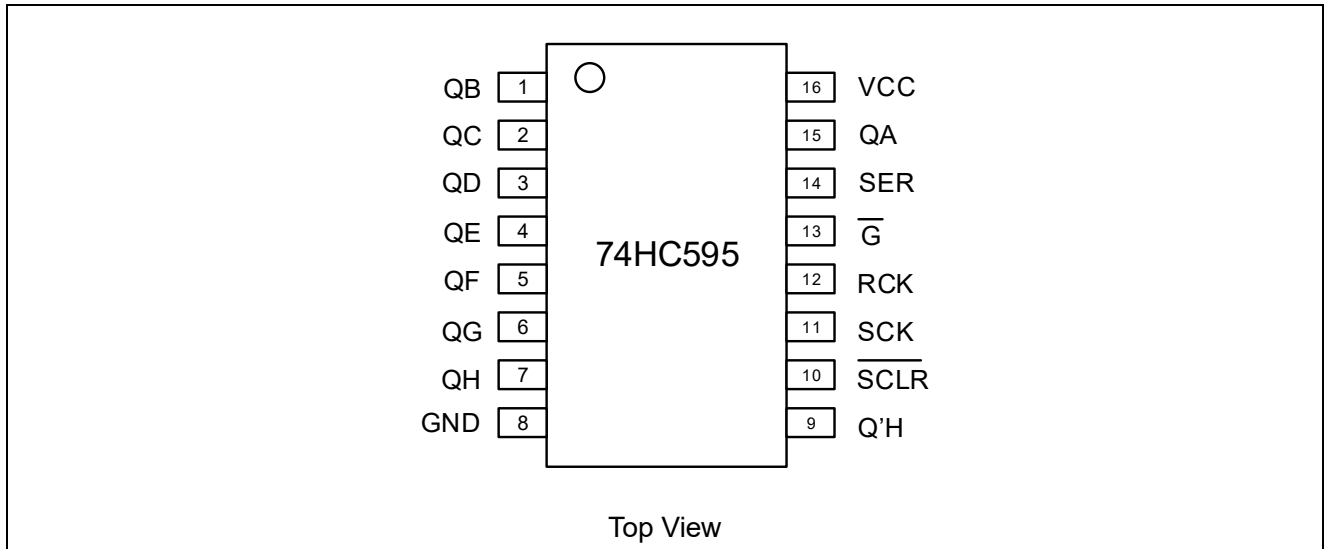
- Low quiescent current: 80 μ A maximum
- Low input current: 1 μ A maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2.0V to 6.0V
- Shift register has direct clear
- Guaranteed shift frequency: DC to 30 MHz

Device information

Part Name	Package
74HC595M	SOP16
74HC595V	TSSOP16

74HC595

Pin Configuration



Pin Function

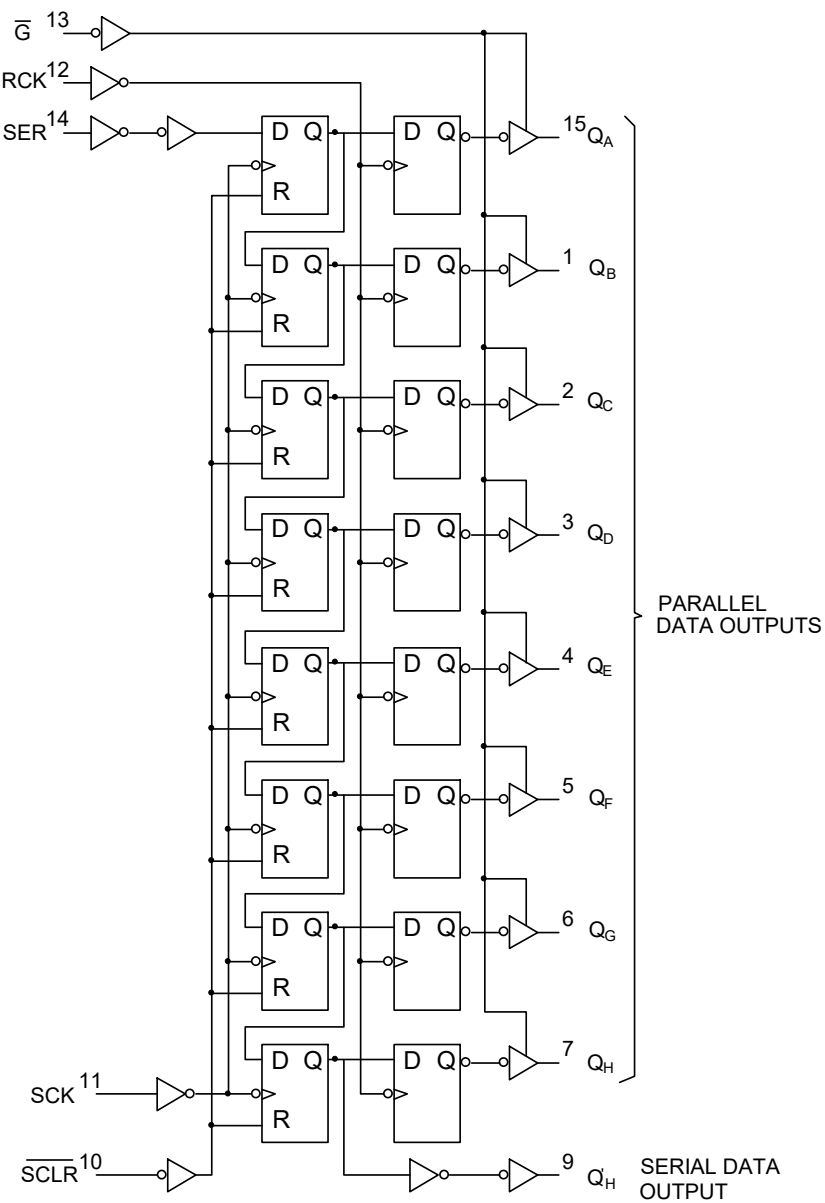
Pin No.	Name	I/O	Description
15, 1~7	QA~QH	O	8 bit 3-STATE Output
8, 16	GND, VCC	—	Ground, Power Supply
9	Q'H	O	Serial Output
10	SCLR	I	Shift Register cleared
11	SCK	I	Shift Register clocked
12	RCK	I	Output Register clocked
13	$\overline{G}$	I	Output state control
14	SER	I	Data input

Truth Table

RCK	SCK	SCLR	$\overline{G}$	Description
X	X	X	H	QA to QH = 3-STATE
X	X	L	L	Shift Register cleared, Q'H = 0
X	↑	H	L	Shift Register clocked, $Q_N = Q_{N-1}$, $Q_0 = SER$
↑	X	H	L	Contents of Shift Register transferred to output latches

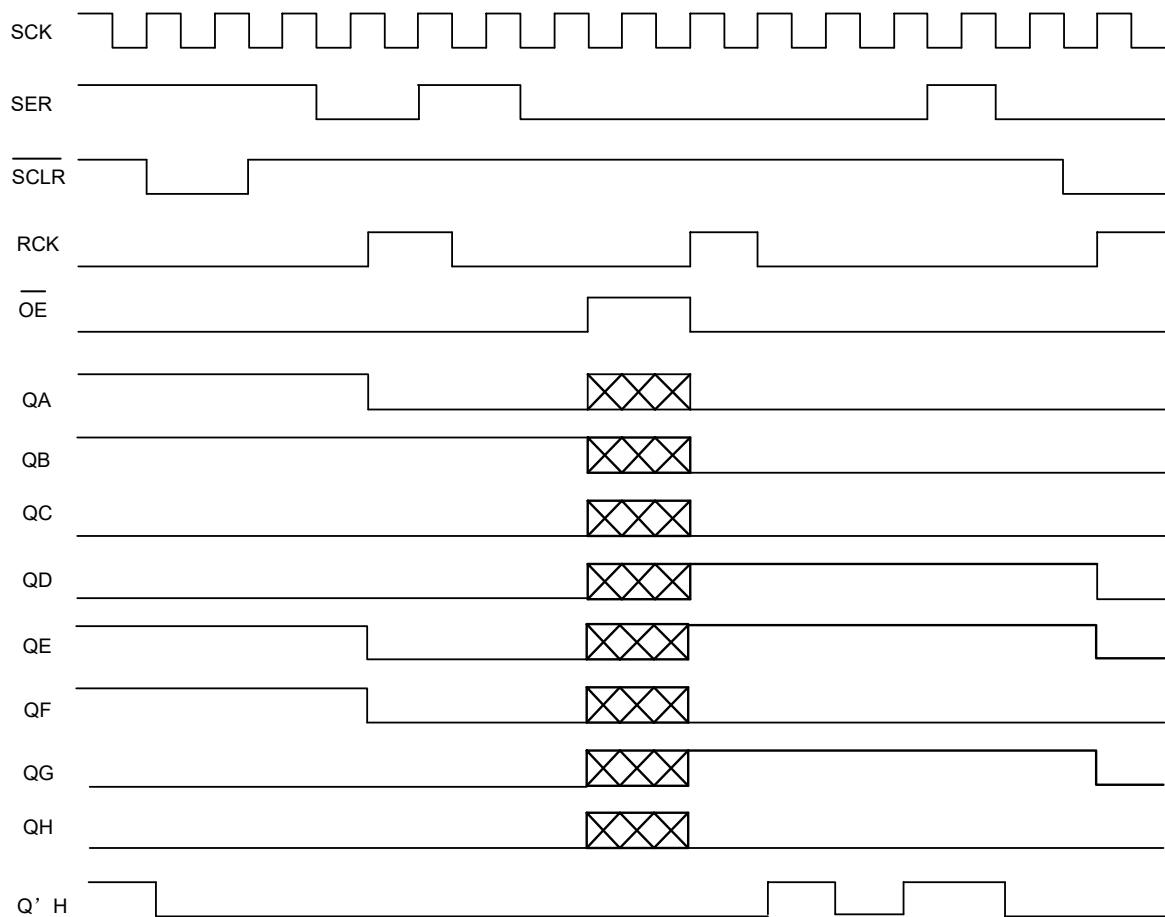
74HC595

Logic Diagram



74HC595

Timing Diagram



NOTE: XXXX implies that the output is in a high-impedance state.

74HC595

Absolute Maximum Ratings

Parameter	Symbol		Value	Unit
Supply Voltage	V _{CC}		-0.5~7.0	V
DC Input Voltage	V _{IN}		-1.5~V _{CC} +1.5	V
DC Output Voltage	V _{OUT}		-0.5~V _{CC} +0.5	V
Input Clamp Current (V _{IN} <0)	I _{IK}		±20	mA
Output Clamp Current (V _{OUT} <0)	I _{OK}		±20	mA
DC Output Current	I _{OUT}		±35	mA
DC V _{CC} or GND Current	I _{CC}		±120	mA
Power Dissipation (T _A = 25°C)	P _D	SOP16	650	mW
		SSOP16	600	
Max Junction Temperature	T _{JMAX}		150	°C
Storage Temperature Range	T _{STG}		-65~150	°C

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply Voltage	V_{CC}		2	6	V
DC Input or Output Voltage	V_{IN} , V_{OUT}		0	V_{CC}	V
Input Rise or Fall Times	t_r , t_f	$V_{CC} = 2.0\text{V}$		1000	ns
		$V_{CC} = 4.5\text{V}$		500	
		$V_{CC} = 6.0\text{V}$		400	
Operating Temperature Range	T_A		-40	+125	°C

74HC595

Electrical Characteristics

DC Characteristics

Symbol	Parameter	Condition	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -40 to 125°C	Unit
				typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage		2V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	
			6V		4.2	4.2	4.2	
V _{IL}	Maximum Low Level Input Voltage		2V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	
			6V		1.8	1.8	1.8	
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤20μA	2V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	
			6V	6	5.9	5.9	5.9	
	Q'H	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤4.0mA	4.5V	4.2	3.98	3.84	3.7	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤5.2mA	6V	5.7	5.48	5.34	5.2	
	QA to QH	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤6.0mA	4.5V	4.2	3.98	3.84	3.7	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤7.8mA	6.0V	5.7	5.48	5.34	5.2	
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤20μA	2V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	
			6V	0	0.1	0.1	0.1	
	Q'H	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤4.0mA	4.5V	0.2	0.26	0.33	0.4	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤5.2mA	6V	0.2	0.26	0.33	0.4	
	QA to QH	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤6.0mA	4.5V	0.2	0.26	0.33	0.4	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤7.8mA	6V	0.2	0.26	0.33	0.4	
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6V		±0.1	±1.0	±1.0	μA
I _{oZ}	Maximum 3-STATE Output Leakage	V _{OUT} = V _{CC} or GND G̅ = V _{IH}	6V		±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0μA	6V		8.0	80	160	μA

74HC595

AC Characteristics ($V_{CC}=2.0\sim 6.0V$, $C_L=50pF$)

Symbol	Parameter	Condition	V _{CC}	T _A = 25°C		T _A = 25 to 85°C	T _A = -40 to 125°C	Unit
				Typ	Guaranteed Limit			
f _{MAX}	Maximum Operating Frequency	C _L =50pF	2V		6	4.8	4.0	MHz
			4.5V		30	24	20	
			6V		35	28	24	
t _{PHL} t _{PLH}	Maximum Propagation Delay from SCK to Q'H	C _L =50pF	2V	58	210	265	315	ns
		C _L =150pF	2V	83	294	367	441	ns
		C _L =50pF	4.5V	14	42	53	63	
		C _L =150pF	4.5V	17	58	74	88	
		C _L =50pF	6V	10	36	45	54	ns
		C _L =150pF	6V	14	50	63	76	
t _{PHL} t _{PLH}	Maximum Propagation Delay from RCK to QA thru QH	C _L =50pF	2V	70	175	220	265	ns
		C _L =150pF	2V	105	245	306	368	ns
		C _L =50pF	4.5V	21	35	44	53	
		C _L =150pF	4.5V	28	49	61	74	
		C _L =50pF	6V	18	30	37	45	ns
		C _L =150pF	6V	26	42	53	63	
t _{PHL}	Maximum Propagation delay from $\overline{\text{SCLR}}$ to Q'H		2V		175	221	261	ns
			4.5V		36	44	52	
			6V		30	37	44	
t _{PZH} t _{PZL}	Maximum Output Enable from $\overline{\text{G}}$ to QA - QH	R _L =1kΩ C _L =50pF	2V	75	175	220	265	ns
		R _L =1kΩ C _L =150pF	2V	100	245	306	368	ns
		C _L =50pF	4.5V	15	35	44	53	
		C _L =150pF	4.5V	20	49	61	74	
		C _L =50pF	6V	13	30	37	45	ns
		C _L =150pF	6V	17	42	53	63	
t _{PHZ} t _{PLZ}	Max Output Disable Time from $\overline{\text{G}}$ to QA -QH	R _L =1kΩ C _L =50pF	2V	75	175	220	265	ns
			4.5V	15	35	44	53	
			6V	13	30	37	45	
t _s	Minimum Setup Time from SER to SCK		2V		100	125	150	ns
			4.5V		20	25	30	
			6V		17	21	25	
t _r	Minimum Removal Time from $\overline{\text{SCLR}}$ to SCK		2V		50	63	75	ns
			4.5V		10	13	15	
			6V		9	11	13	

74HC595

AC Characteristics Continued ($V_{CC} = 2.0 \sim 6.0V$, $C_L = 50pF$)

Symbol	Parameter	Condition	V _{CC}	T _A = 25°C		T _A = 25 to 85°C	T _A = -40 to 125°C	Unit
				Typ	Guaranteed Limit			
t _s	Minimum Setup Time from SCK to RCK		2V		100	125	150	ns
			4.5V		20	25	30	
			6V		17	21	26	
t _H	Minimum Hold Time SER to SCK		2V		5	5	5	ns
			4.5V		5	5	5	
			6V		5	5	5	
t _w	Minimum Pulse Width of SCK or $\overline{\text{SCLR}}$		2V	30	80	100	120	ns
			4.5V	9	16	20	24	
			6V	8	14	18	22	
t _r t _f	Maximum Input Rise and Fall Time, Clock		2V		1000	1000	1000	ns
			4.5V		500	500	500	
			6V		400	400	400	
t _{THL} t _{TLH}	Maximum Output Rise and Fall Time QA–QH		2V	25	60	75	90	ns
			4.5V	7	12	15	18	
			6V	6	10	13	15	
t _{THL} t _{TLH}	Max Output Rise & Fall Time Q'H		2V		75	95	110	ns
			4.5V		21	25	28	
			6V		19	22	25	
C _{PD}	Power Dissipation Capacitance, Outputs Enable	f=1MHz, $\overline{\text{G}}$ =V _{CC}		90				pF
		f=1MHz, $\overline{\text{G}}$ =GND		150				
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF
C _{OUT}	Maximum Output Capacitance			15	20	20	20	pF

74HC595

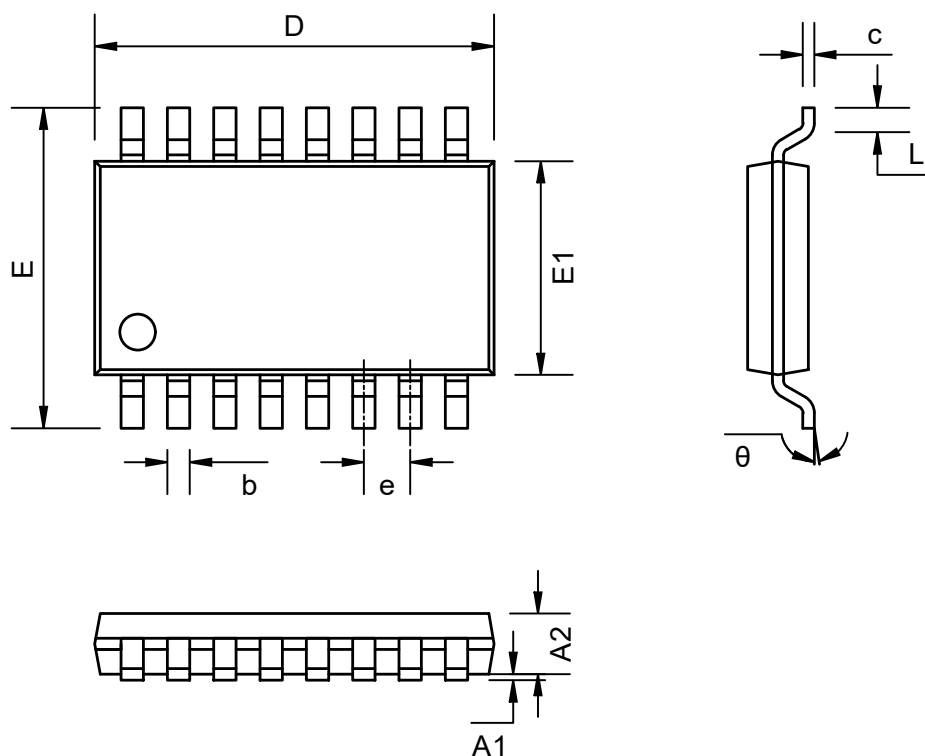
Timing Characteristics ($V_{CC} = 5V$, $T_A = 25^\circ C$)

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MAX}	Max Operating Frequency of SCK			30	MHz
$t_{PHL} \ t_{PLH}$	Max Propagation Delay, SCK to Q'H	$C_L = 45pF$	22	32	ns
$t_{PHL} \ t_{PLH}$	Max Propagation Delay, RCK to QA thru QH	$C_L = 45pF$	18	30	ns
$t_{PZH} \ t_{PZL}$	Max Output Enable Time from G to QA thru QH	$R_L = 1k\Omega$ $C_L = 45pF$	17	28	ns
$t_{PHZ} \ t_{PLZ}$	Max Output Disable Time from $\overline{G}$ to QA to QH	$R_L = 1k\Omega$ $C_L = 5pF$	15	25	ns
t_s	Min Setup Time from SER to SCK			20	ns
t_s	Min Setup Time from SCLR to SCK			20	ns
t_s	Min Setup Time from SCK to RCK			40	ns
t_H	Min Hold Time from SER to SCK			0	ns
t_w	Min Pulse Width of SCK or RCK			16	ns

74HC595

Package Dimension

SOP16

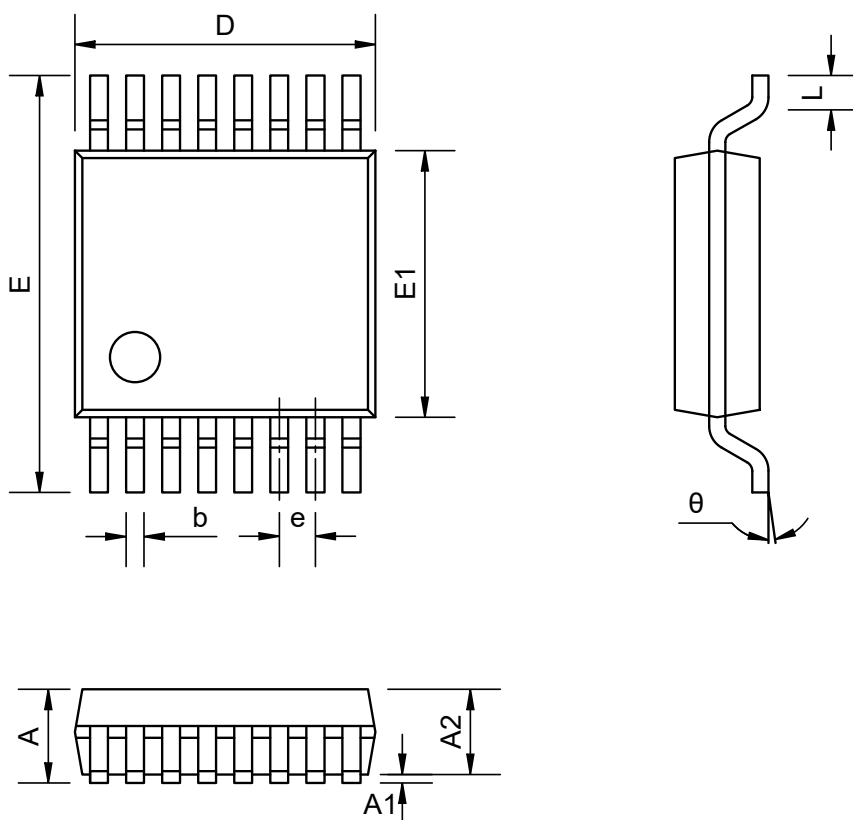


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A1	0.10	0.20	0.30
A2	1.35	1.45	1.55
b	0.306	0.406	0.506
c	--	0.203	--
D	9.90	10.00	10.10
E	5.84	6.04	6.24
E1	3.85	3.95	4.05
e	1.27BSC		
L	0.35	0.55	0.75
θ	2°	--	8°

74HC595

TSSOP16



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	--	1.05
b	0.20	--	0.28
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
θ	0°	--	8°

74HC595

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2015-09-11	Initial Version	Wuxj	Wuxj	Zhujl
1.1	2019-01-08	Add T _J	Wuxj	Wuxj	Liujiy
1.2	2022-07-22	Update typeset	Shibo	Shibo	Zhujl
1.3	2024-05-11	ICC max up to 120mA	Shibo	Shibo	Shibo