

# **Octal Buffers/Drivers With 3-State Outputs**

### **General Description**

The ET74LV541V octal buffers/drivers is ideal for driving bus lines or buffer memory address registers. The device feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide non-inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### **Features**

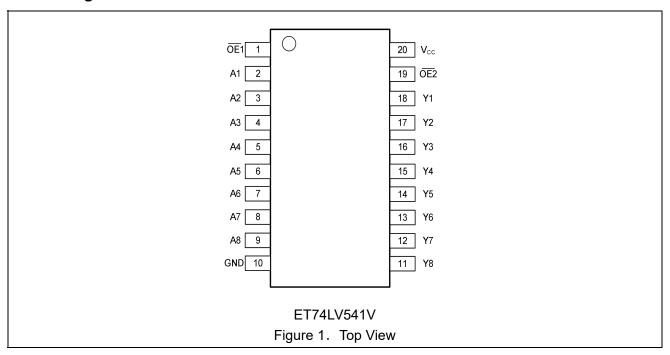
- Designed for 2 to 5.5V V<sub>CC</sub> Operation
- Inputs are TTL Voltage Compatible
- Max t<sub>pd</sub> of 6ns at 5V
- ESD Protection:
  - --HBM JESD22-A114-A Exceeds 2000 V
  - --CDM JESD22-C101-A Exceeds 1500 V
- Latch-up Performance Exceeds 200 mA
- Part No. and package

Part No.	Package	MSL
ET74LV541V	TSSOP20 (6.5mm×4.4mm)	3

### **Applications**

- Fully compliant with standards for automotive applications
- Combine normal power signals from multiple power rails

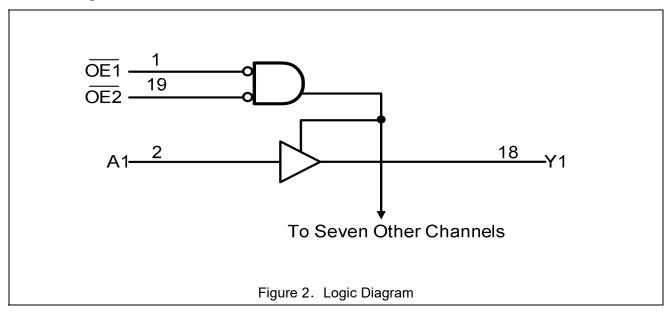
# Pin Configuration



### **Pin Function**

Pin No.	Name	Description
1	OE 1	Output Enable 1
2	A1	Input A1
3	A2	Input A2
4	A3	Input A3
5	A4	Input A4
6	A5	Input A5
7	A6	Input A6
8	A7	Input A7
9	A8	Input A8
10	GND	Ground
11	Y8	Output Y8
12	Y7	Output Y7
13	Y6	Output Y6
14	Y5	Output Y5
15	Y4	Output Y4
16	Y3	Output Y3
17	Y2	Output Y2
18	Y1	Output Y1
19	OE 2	Output Enable 2
20	Vcc	Power

# **Block Diagram**



## **Functional Description**

### **Function Table**

	Output		
OE1	OE2	A	Υ
L	L	L	L
L	L	Н	Н
Н	X	X	Z
X	Н	X	Z

**Note**: H = High voltage level

L = Low voltage level

X = Don't care

Z = High-impedance OFF-state

### **Absolute Maximum Ratings**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Value	Unit
V <sub>CC</sub>	DC Supply Voltage		-0.5 to 7.0	V
Vı	Input Voltage <sup>(1)</sup>		-0.5 to 7.0	V
1/	Output Voltage <sup>(1)</sup> (2)		-0.5 to 7.0	V
Vo	Output Voltage(**/		-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Clamp Current	V <sub>I</sub> < GND	-20	mA
lok	Output Clamp Current	Vo< GND	-50	mA
lo	Output Current	I <sub>O</sub> (V <sub>O</sub> =0 to V <sub>CC</sub> )	±35	mA
Icc	Supply Current		±70	mA
$I_{GND}$	Ground Current		±70	mA
T <sub>JMAX</sub>	Maximum Junction Temperature		150	°C
$P_D$	Max Power Dissipation	TSSOP20	400	mW
T <sub>STG</sub>	Storage Temperature Range		-65 to 150	°C
\ <u>'</u>	НВМ	Per JESD22-A114-A	±2000	V
V <sub>ESD</sub>	CDM	Per JESD22-C101-A	±1500	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
I <sub>LU</sub>	Max Latch up Current	Per EIA/JESD78E	±200	mA

**Note1**. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

Note2. This value is limited to 5.5V maximum.

# **Recommended Operating Conditions**

Symbol	Par	Min	Max	Unit		
V <sub>CC</sub>	Supp	oly voltage	2.0	5.5	V	
		V <sub>CC</sub> =2V	1.5		V	
N/	High lavel input valtage	V <sub>CC</sub> =2.3V to 2.7V	V <sub>CC</sub> *0.7			
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> =3V to 3.6V	V <sub>CC</sub> *0.7			
		V <sub>CC</sub> =4.5V to 5.5V	V <sub>CC</sub> *0.7			
		V <sub>CC</sub> =2V		0.5	V	
N/	Lave lavel inner treeltage	V <sub>CC</sub> =2.3V to 2.7V		V <sub>CC</sub> *0.3		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> =3V to 3.6V		V <sub>CC</sub> *0.3		
		V <sub>CC</sub> =4.5V to 5.5V		V <sub>CC</sub> *0.3		
Vı	Inpu	ut Voltage	0	5.5	V	
Vo	Outp	out Voltage	0	Vcc	V	
		V <sub>CC</sub> =2V		-50	uA	
,	I Park I and a standard annual	V <sub>CC</sub> =2.3V to 2.7V		-2	mA	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> =3V to 3.6V		-8	mA	
		V <sub>CC</sub> =4.5V to 5.5V		-16	mA	
		V <sub>CC</sub> =2V		50	uA	
,	1 1 4 4	V <sub>CC</sub> =2.3V to 2.7V		2	mA	
lol	Low-level output current	V <sub>CC</sub> =3V to 3.6V		8	mA	
		V <sub>CC</sub> =4.5V to 5.5V		16	mA	
T <sub>A</sub>	Operating Ter	erating Temperature Range		125	°C	
	land Tanakita	V <sub>CC</sub> =2.3V to 2.7V		200		
Δt/ΔV	Input Transition	V <sub>CC</sub> =3V to 3.6V		100	ns/V	
	rise or fall rate	V <sub>CC</sub> =4.5V to 5.5V		20	1	

# **Electrical Characteristics**

### **DC Electrical Characteristics**

Cumbal	T <sub>A</sub> =25°C			-40°C≤T	մ≤125°C	11:4:4			
Symbol	Parameter	Condition	V <sub>cc</sub> (V)	Min	Тур	Max	Min	Max	Unit
		I <sub>OH</sub> =-50uA	2 to 5.5	V <sub>CC</sub> -0.1	4.5		V <sub>CC</sub> -0.1		
\ \/	High-Level	I <sub>OH</sub> =-2mA	2.3	2			2		<sub>v</sub>
V <sub>ОН</sub>	Output Voltage	I <sub>OH</sub> =-8mA	3	2.48			2.48		V
		Іон=-16mA	4.5	3.8			3.8		
		I <sub>OL</sub> =50uA	2 to 5.5			0.1		0.1	
	Low-Level	I <sub>OL</sub> =2mA	2.3			0.4		0.4	<sub>v</sub>
Vol	Output Voltage	I <sub>OL</sub> =8mA	3			0.44		0.44	
		I <sub>OL</sub> =16mA	4.5			0.55		0.55	
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> =5.5V or GND	0 to 5.5			±1		±1	
l <sub>OZ</sub>	Output Leakage Current	Vo=V <sub>CC</sub> or GND	5.5			±5		±5	uA
Icc	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5			20		20	μA
l <sub>off</sub>	Power-off Leakage Current	$V_1$ or $V_0 = 0$ to 5.5V	0			5		5	uA
Ci	V <sub>I</sub> =V <sub>CC</sub> or	GND	3.3		2				pF

# Switching Characteristics (3)

Cumbal	Condition		T <sub>A</sub> =2	T <sub>A</sub> =25°C		-40°C≤T <sub>A</sub> ≤125°C		
Symbol	Conc	illon	Тур	Max	Min	Тур	Max	Unit
	From A to Y,	V <sub>CC</sub> =2.5V	6.7	11.3	1.0		13.5	
	C <sub>L</sub> =15pF	V <sub>CC</sub> =3.3V	4.8	7.0	1.0		8.5	
<b>.</b>	OL-13pF	V <sub>CC</sub> =5V	3.5	5	1.0		6	
t <sub>pd</sub>	Fram A to V	V <sub>CC</sub> =2.5V	8.7	15.9	1.0		18.5	
	From A to Y, $C_L$ =50pF	V <sub>CC</sub> =3.3V	6.1	10.5	1.0		12	
	CL-50PF	V <sub>CC</sub> =5V	4.3	7.0	1.0		8.0	no
	Fram /OF to V	V <sub>CC</sub> =2.5V	8.5	16.6	1.0		19.5	ns
	From /OE to Y, $C_L=15pF$	V <sub>CC</sub> =3.3V	6.1	10.5	1.0		12.5	
4	CL=15pr	V <sub>CC</sub> =5V	4.3	7.2	1.0		8.5	
t <sub>en</sub>	Fram /OF to V	V <sub>CC</sub> =2.5V	10.5	20.7	1.0		24	
	From /OE to Y,	V <sub>CC</sub> =3.3V	7.4	14	1.0		16	
	C <sub>L</sub> =50pF	V <sub>CC</sub> =5V	5.3	9.2	1.0		10.5	

## Switching Characteristics (Continued) (3)

Cumbal	Condition		T <sub>A</sub> =2	T <sub>A</sub> =25°C		-40°C≤T <sub>A</sub> ≤125°C		
Symbol	Cond	ition	Тур	Max	Min	Тур	Max	Unit
	From IOF to V	V <sub>CC</sub> =2.5V	8.4	13.1	1.0		15	
	From /OE to Y, C <sub>L</sub> =15pF	Vcc=3.3V	5.8	11	1.0		12	
<b>+</b>	CL=15PF	V <sub>CC</sub> =5V	3.9	7.5	1.0		8	
t <sub>dis</sub>	5 /OF to V	V <sub>CC</sub> =2.5V	12.3	17.9	1.0		20	
	From /OE to Y,	V <sub>CC</sub> =3.3V	8.8	15.4	1.0		17.5	ns
	C∟=50pF	V <sub>CC</sub> =5V	5.6	8.8	1.0		10	
	V <sub>CC</sub> =2	2.5V		2			2	
T <sub>sk(o)</sub>	V <sub>CC</sub> =	3.3V		1.5			1.5	]
	V <sub>CC</sub> =	=5V		1			1	]

Note3. Guaranteed by design and characterization. not a FT item.

#### Noise Characteristics(4)

 $V_{CC} = 3.3 \text{ V}, C_L = 50 \text{pF}, T_A = 25^{\circ}\text{C}$ 

Symbol	Parameter	Min	Тур	Max	Unit
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.5	0.8	V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.4	-0.8	V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		2.9		V
V <sub>IH(D)</sub>	High-level dynamic input voltage	2.31			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.99	V

Note4. Characteristics are for surface-mount packages only.

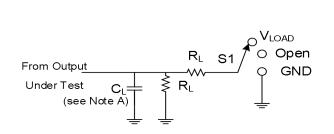
### Operating Characteristics<sup>(5)</sup>

 $T_A = 25^{\circ}C$ 

Symbol	Parameter		Conditions		Тур	Unit
	Power dissipation	Outpute enabled	C <sub>L</sub> = 50pF,	V <sub>CC</sub> =3.3 V	16.3	_
Cpd	capacitance	Outputs enabled	f =10 MHz	V <sub>CC</sub> =5 V	17.8	pF

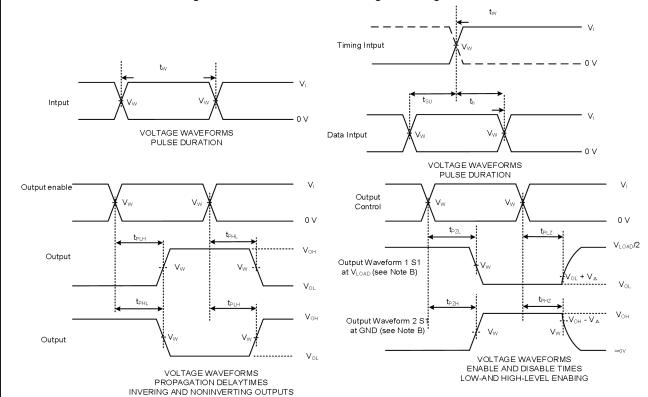
 $\textit{Note5.}\ C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

#### **AC Characteristics Test Waveform**



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	$V_{LOAD}$
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

Figure.3 Test circuit for measuring switching times



#### Notes:

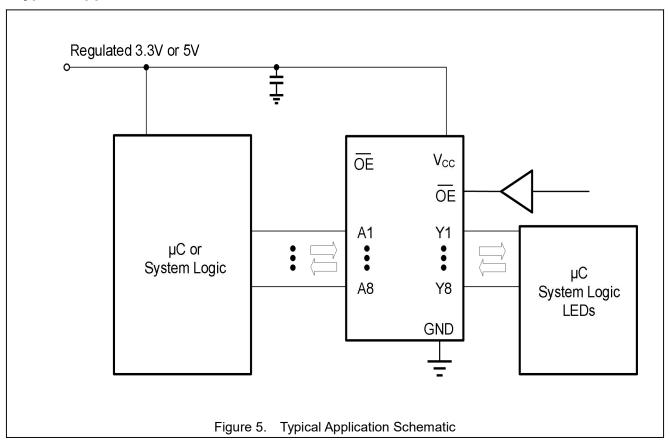
- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
- C. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- D. All input pulses are supplied by generators having the following characteristics:

PRR  $\leq$ 10 MHz,  $Z_O = 50 \Omega$ 

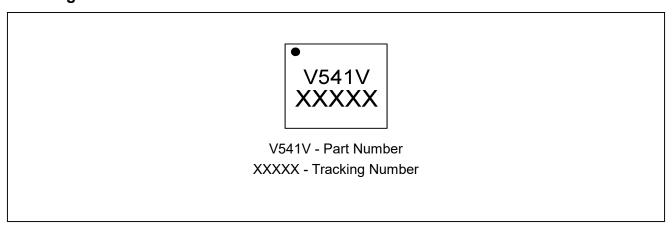
- E. The outputs are measured one at a time, with one transition per measurement.
- F. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- G. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- I. All parameters and waveforms are not applicable to all devices.

Figure.4 Input to output propagation delay times

# **Typical Application**

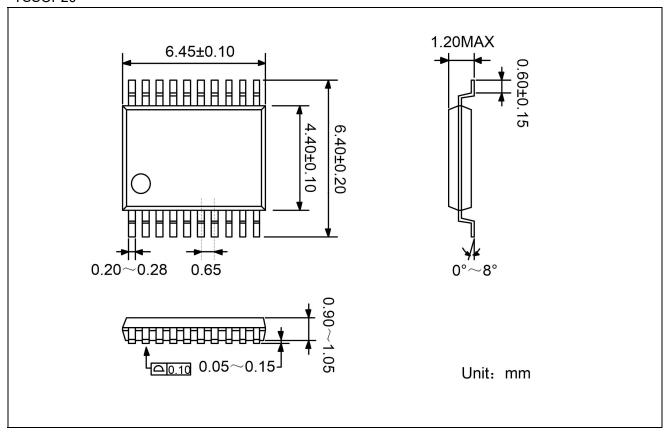


## Marking



# **Package Dimension**

### TSSOP20



## **Revision History and Checking Table**

Version	Date	Revision Item	Modifier	Function & Spec	Package & Tape
				Checking	Checking
0.0	2023-12-20	Initial version	Shibo	Luh	Liujy
1.0	2025-6-20	Official Version	Lizihao	Yangxx	Liujy