Linear Li-Ion Battery Charger IC

General Description

ET95101 is a high performance devices for space limited portable applications highly integrated Li-Ion battery linear charger. The high input voltage range with input over-voltage protection supports low cost, non regulated adapters. The ET95101 has a power output that can charge the battery. If the average system load cannot fully charge the battery during the 10 hours security timer, you can parallel the system load with the battery.

The battery charging goes through the following three stages: regulation(pre-charge), constant current(CC) and constant voltage(CV).In all charging stages, the internal control loop will monitor the IC junction temperature, and when it exceeds the internal temperature threshold, it will reduce the charging current.

The charger power level and charging current sensing functions are fully integrated. The charger has high-precision current and voltage regulation loop and charging termination function. The charging current value can be programmed via an external resistor.

Features

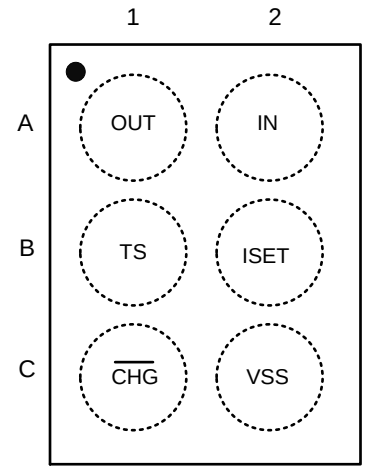
- 1% charging voltage accuracy
- 10% charging current accuracy
- Support the application of ultra-low charging current (10mA to 250mA)
- Support minimum 1mA charging termination current
- Ultra low battery output leakage current: 75nA (maximum)
- 30V rated input voltage; With 6.5 V input over-voltage protection
- Input voltage dynamic power management
- 120 °C thermal conditioning; 150 °C thermal shutdown protection
- OUT short-circuit protection and ISET short-circuit detection
- Operating within JEITA range through battery negative temperature coefficient (NTC)—fast charging current in case of cold fault is halved, and voltage in case of hot fault is 4.06V
- Fixed 10 hours safety timer
- Automatic termination and timer disable mode for missing battery pack(TTDM)
- Package information:

Part No.	Package	MSL
ET95101	CSP6(1.30 mm * 0.9 mm)	Level 1

Application

- Fitness Accessories
- Smart watch
- Bluetooth Headphones
- Low-power consumption of handheld devices

Pin Configuration

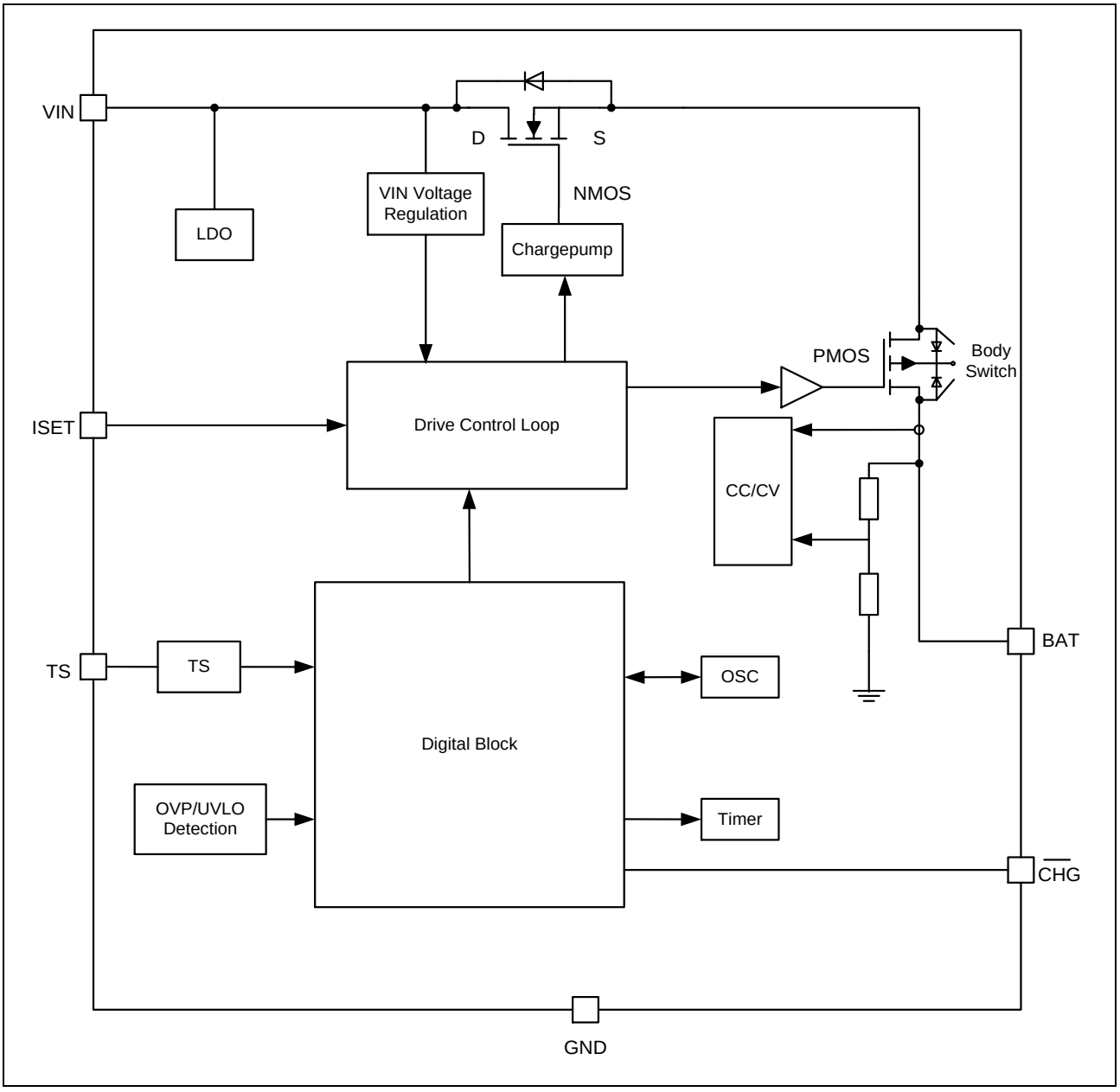


ET95101 Top View

Pin Function

Pin No.	Name	Function
A1	OUT	Battery Charge Current Output. Power Supply Input.
A2	IN	Power Supply Input.
B1	TS	Temperature sense pin connected to 10k at 25°C NTC thermistor, in the battery pack. Floating TS pin or pulling high puts part in TTDM “Charger” mode and disables TS monitoring, Timers and Termination. Pulling pin low disables the IC. If NTC sensing is not needed, connect this pin to VSS through an external 10kΩ resistor. A 250kΩ resistor from TS to ground will prevent IC entering TTDM mode when battery with thermistor is removed.
B2	ISET	Programs the fast-charge current setting. External resistor from ISET to VSS defines fast charge current value. Recommended range is 13.5kΩ(10mA) to 0.54kΩ(250mA).
C1	$\overline{\text{CHG}}$	Low(FET on) indicates charging and open drain (FET off) indicates no charging or the first charge cycle complete.
C2	VSS	Ground Pin.

Block Diagram



Functional Description

The ET95101 is a highly integrated of single cell Li-Ion charger. The charger can be used to charge a battery, power a system or both. The charger has three phases of charging: pre-charge to recover a fully discharged battery, fast-charge constant current to supply the charge safely and voltage regulation to safely reach full capacity. The charger is very flexible, allowing programming of the fast-charge current and pre-charge/Termination Current. This charger is designed to work with a USB connection (100mA limit) or Adaptor (DC output). The charger also checks to see if a battery is present.

The charger also comes with a full set of safety features: JEITA Temperature Standard, Over-Voltage protection, DPM-IN, Safety Timers, and ISET short protection. All of these features and more are described in detail below.

The charger is designed for a single power path from the input to the output to charge a single cell Li-Ion or Li-Pol battery pack. Upon application of a 5V DC power source the ISET and OUT short checks are performed to assure a proper charge cycle.

If the battery voltage is below the LOWV threshold, the battery is considered discharged and a preconditioning cycle begins. The termination "current threshold" is always half of the pre-charge programmed current level.

Once the battery voltage has charged to the VLOWV threshold, fast charge is initiated and the fast charge current is applied. The fast charge constant current is programmed using the ISET pin. The constant current provides the bulk of the charge. Power dissipation in the IC is greatest in fast charge with a lower battery voltage. If the IC reaches 120°C, the IC enters thermal regulation, slows the timer clock by half, and reduces the charge current as needed to keep the temperature from rising any further. Figure 1 shows the charging profile with thermal regulation. Typically under normal operating conditions, the IC’s junction temperature is less than 120°C and thermal regulation is not entered.

Once the cell has charged to the regulation voltage the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold. The termination can be disabled if desired. Further details are described in the Operating Modes section.

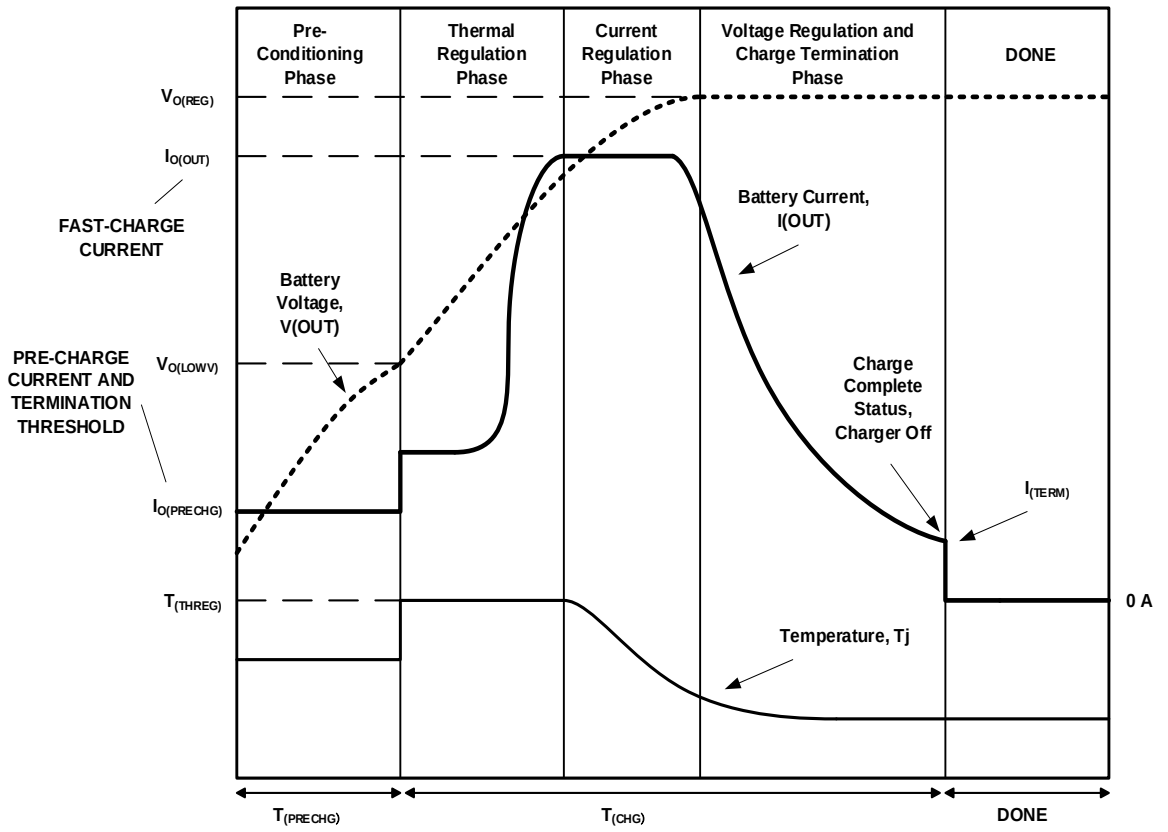


Figure 1 Charging Profile with Thermal Regulation

VIN Over-Voltage Protection (OVP)

If the input source applies an over-voltage, the pass FET, if previously on, turns off after a deglitch, $T_{BLK(OVP)}$. The timer stops counting. Once the over-voltage returns to a normal voltage, the timer and charge continues.

$\overline{CHG}$ Pin Indication

The charge pin has an internal open drain FET which is on (pulls down to VSS) during the first charge only (independent of TTDM) and is turned off once the battery reaches voltage regulation and the charge current tapers to the termination threshold. The ET95101 terminates at 9% of the programmed charge current. The charge pin is high impedance in sleep mode and OVP and returns to its previous state once the condition is removed. Cycling input power, removing and replacing the battery, pulling the TS pin low and releasing or entering pre-charge mode causes the $\overline{CHG}$ pin to go reset (go low if power is good and a discharged battery is attached) and is considered the start of a first charge.

$\overline{CHG}$ Pin LED Pull-up Source

For host monitoring, a pull-up resistor is used between the $\overline{CHG}$ pin and the VCC of the host and for a visual indication a resistor in series with an LED is connected between the $\overline{CHG}$ pin and a power source. If the $\overline{CHG}$ source is capable of exceeding 7 V, a 6.2-V zener should be used to clamp the voltage. If the source is the OUT pin, note that as the battery changes voltage, and the brightness of the LEDs vary.

IN-DPM

The IN-DPM feature is used to detect an input source voltage that is folding back (voltage dropping), reaching its current limit due to excessive load. When the input voltage drops to the V_{IN-DPM} threshold the internal pass FET starts to reduce the current until there is no further drop in voltage at the input. This would prevent a source with voltage less than V_{IN-DPM} to power the out pin. This is an added safety feature that helps protect the source from excessive loads.

OUT

The Charger's OUT pin provides current to the battery and to the system, if present. This IC can be used to charge the battery plus power the system, charge just the battery or just power the system (TTDM) assuming the loads do not exceed the available current. The OUT pin is a current limited source and is inherently protected against shorts. If the system load ever exceeds the output programmed current threshold, the output will be discharged unless there is sufficient capacitance or a charged battery present to supplement the excessive load.

ISET

An external resistor is used to Program the Output Current (10 to 250 mA) and can be used as a current monitor.

$$R_{ISET} = K_{ISET} \div I_{OUT}$$

Where:

I_{OUT} is the desired fast charge current;

K_{ISET} is a gain factor found in the electrical specification

For greater accuracy at lower currents, part of the sense FET is disabled to give better resolution. Going from higher currents to low currents, there is hysteresis and the transition occurs around 50mA.

The ISET resistor is short protected and will detect a resistance lower than ≈420Ω. The detection requires at least 50mA of output current. If a "short" is detected, then the IC will latch off and can be reset by cycling the power or cycling TS pin. The OUT current is internally clamped to a maximum current of 600mA typical and is independent of the ISET short detection circuitry.

For charge current that is below 50mA, an extra RC circuit is recommended on ISET to achieve more stable current signal.

TS

The TS function for the ET95101 is designed to follow the new JEITA temperature standard for Li-Ion batteries. There are now four thresholds, 60°C, 45°C, 10°C, and 0°C. Normal operation occurs between 10°C and 45°C. If between 0°C and 10°C the charge current level is cut in half and if between 45°C and 60°C the regulation voltage is reduced to 4.06V. See figure 2.

The TS feature is implemented using an internal 50μA current source to bias the thermistor (designed for use with a 10kΩ NTC β = 3370 (SEMITEC 103AT-2 or Mitsubishi TH05-3H103F) connected from the TS pin to

V_{SS}. If this feature is not needed, a fixed 10kΩ can be placed between TS and V_{SS} to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS pin low to disable charge.

The TS pin has two additional features, when the TS pin is pulled low or floated/driven high. A low disables charge and a high puts the charger in TTDM.

Above 60°C or below 0°C the charge is disabled. Once the thermistor reaches -10°C the TS current folds back to keep a cold thermistor (between -10°C and -50°C) from placing the IC in the TTDM mode. If the TS pin is pulled low into disable mode, the current is reduced to 30μA. Since the I_{TS} current is fixed along with the temperature thresholds, it is not possible to use thermistor values other than the 10kΩ NTC (at 25°C).

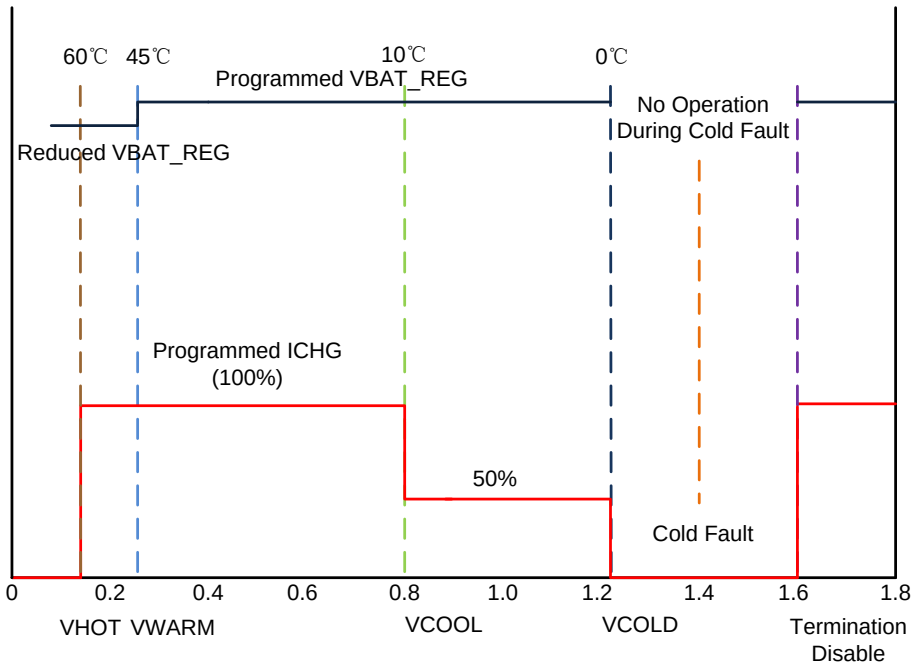


Figure 2 TS Voltage-V

Timers

The pre-charge timer is set to 30 minutes. The pre-charge current, can be programmed to off-set any system load, making sure that the 30 minutes is adequate.

The fast charge timer is fixed at 10 hours and can be increased real time by going into thermal regulation or IN-DPM. The timer clock slows by a factor of 2, resulting in a clock than counts half as fast when in these modes. If either the 30 minute or ten hour timer times out, the charging is terminated and for ET95101 the $\overline{CHG}$ pin goes high impedance if not already in that state. The timer is reset by disabling the IC, cycling power or going into and out of TTDM.

Termination

Once the OUT pin goes above V_{RCH}, (reaches voltage regulation) and the current tapers down to the termination threshold, a battery detect route is run to determine if the battery was removed or the battery is full.If the battery is present, the charge current will terminate. If the battery was removed along with the thermistor, then the TS pin is driven high and the charge enters TTDM. If the battery was removed and the TS pin is held in the active region, then the battery detect routine will continue until a battery is inserted.

Power-Down or Under-voltage Lockout (UVLO)

The ET95101 is in power down mode if the IN pin voltage is less than UVLO. The part is considered “dead” and all the pins are high impedance. Once the IN voltage rises above the UVLO threshold the IC will enter Sleep Mode or Active mode depending on the OUT pin (battery) voltage.

Power-up

The IC is alive after the IN voltage ramps above UVLO (see sleep mode), resets all logic and timers, and starts to perform many of the continuous monitoring routines. Typically the input voltage quickly rises through the UVLO and sleep states where the IC declares power good, starts the qualification charge at 22mA, sets the charge current base on the ISET pin, and starts the safety timer.

Sleep Mode

If the IN pin voltage is between $V_{OUT}+V_{DT}$ and UVLO, the charge current is disabled, the safety timer counting stops (not reset). As the input voltage rises and the charger exits sleep mode, the safety timer continues to count and the charge is enabled. See figure3.

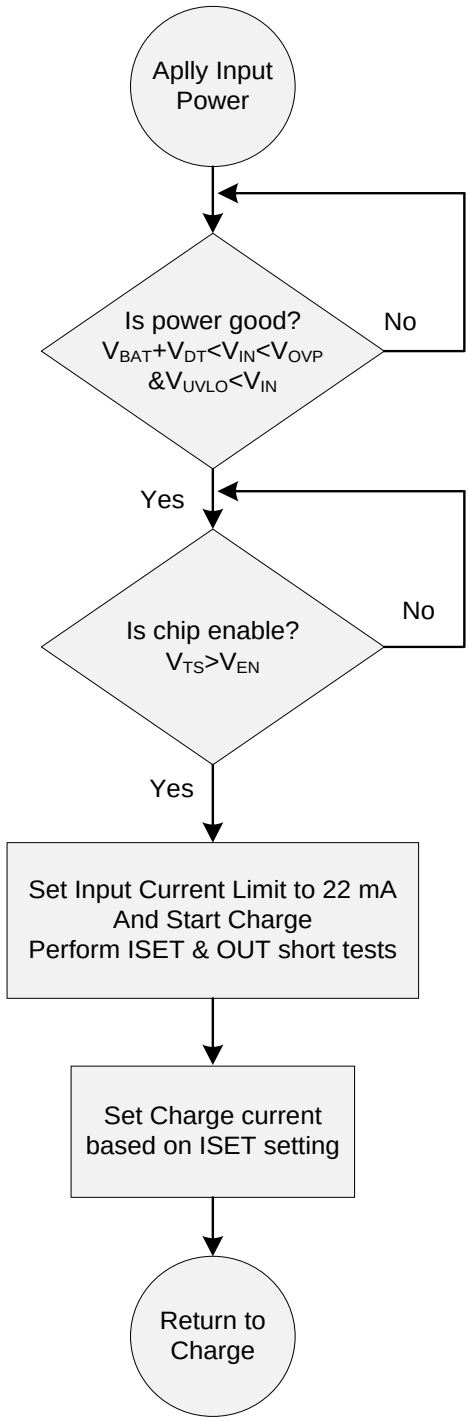


Figure 3 Power-Up Flow Diagram

New Charge Cycle

A new charge cycle is started when a good power source is applied, performing a chip disable/enable (TS pin), exiting Termination and Timer Disable Mode (TTDM), detecting a battery insertion or the OUT voltage dropping below the V_{RCH} threshold.

Termination and Timer Disable Mode (TTDM) - TS Pin High

The battery charger is in TTDM when the TS pin goes high from removing the thermistor (removing battery pack/floating the TS pin) or by pulling the TS pin up to the TTDM threshold.

When entering TTDM, safety timer is reset and disabled, termination is also disabled. A battery detect routine is run to see if the battery was removed or not. For ET95101, if the battery was removed then the $\overline{CHG}$ pin will go to its high impedance state if not already there. If a battery is detected the $\overline{CHG}$ pin does not change states until the current tapers to the termination threshold, where the $\overline{CHG}$ pin goes to its high impedance state if not already there (the regulated output will remain on).

The charging profile does not change (still has pre-charge, fast-charge constant current and constant voltage modes). This implies the battery is still charged safely and the current is allowed to taper to zero.

When coming out of TTDM, if a battery is detected, then a new charge cycle begins.

If TTDM is not desired upon removing the battery with the thermistor, one can add a 237kΩ resistor between TS and VSS to disable TTDM. This keeps the current source from driving the TS pin into TTDM. This creates≈0.1°C error at hot and a ≈3°C error at cold.

Battery Detect Routine

The battery detect routine should check for a missing battery while keeping the OUT pin at a useable voltage. The battery detect routine is run when entering TTDM to verify if battery is present, or run all the time if battery is missing and not in TTDM. On power-up, if battery voltage is greater than V_{RCH} threshold and charge termination, a battery detect routine is run to determine if a battery is present.

The battery detect routine is disabled while the IC is in TTDM, or has a TS fault. See figure 4 for the Battery Detect Flow Diagram.

Refresh Threshold

After termination, if the OUT pin voltage drops to V_{RCH} (100mV below regulation) then a new charge is initiated.

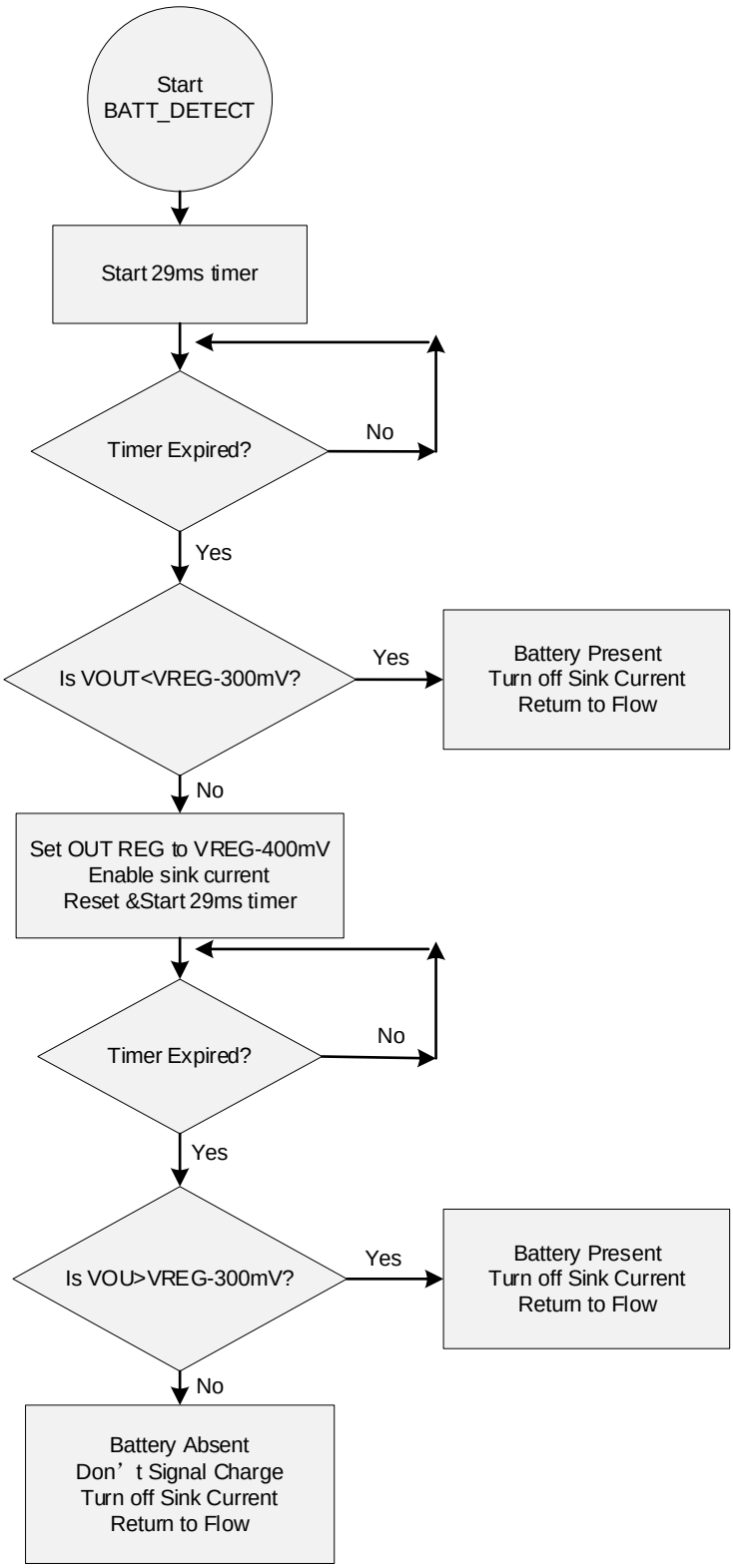


Figure 4 Battery Detect Routine

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

Parameter	Rating	Unit
Supply Input Voltage, VIN	-0.3~30	V
Other Pins	-0.3~6	V
Input Current	300	mA
Output Current	300	mA
Output Sink Current	15	mA
Junction temperature	-40~150	°C

Recommended Operating Conditions (Refer to the typical application circuit)

Parameter	Range	Unit
Supply Input Voltage, VIN	3.5~28	V
IN operating voltage range	4.45~6.45	V
Junction Temperature Range	0~125	°C
Input current, IN pin, I_{IN}	250	mA
Current, OUT pin, I_{OUT}	250	mA
Fast-charge current programming resistor, R_{ISET}	0.54~13.5	kΩ
10kΩ NTC thermistor range without entering $\overline{BAT\_EN}$ or TTDM	1.66~258	kΩ

Electrical Characteristics

Unless otherwise noted, typical values are at V_{IN}=5V, V_{OUT}=4V, T_A=25°C.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
INPUT						
V_{UVLO}	Under Voltage lock-out exit	V_{IN}: 0 V → 4 V	3.15	3.3	3.45	V
V_{HYS_UVLO}	Hysteresis on V_{UVLO_RISE} falling	V_{IN}: 4 V→0 V; V_{UVLO_FALL} = V_{UVLO_RISE} - $V_{HYS-UVLO}$		250		mV
T_{DGL} (UVLO_NO)	Deglitch time on exiting UVLO	Time measured from V_{IN}: 0 V → 5 V to charge enable; V_{OUT} = 3.6 V		29		ms
V_{IN-DT}	Input power good detection threshold is V_{OUT} + V_{IN-DT}	Input power good if V_{IN}> V_{OUT} + V_{IN-DT}; V_{OUT} = 3.6 V; V_{IN}: 3.5 V → 4 V	15	60	130	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT} falling	V_{OUT} = 3.6 V; V_{IN}: 4 V → 3.5 V		30		mV
V_{OVP}	Input over-voltage protection threshold	V_{IN}: 5 V → 12 V	6.50	6.65	6.8	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{IN}: 11 V → 5 V		110		mV
$T_{BLK(OVP)}$	Input over-voltage blanking time	V_{IN}: 5 V → 12 V		1		us
$T_{DGL(OVP-REC)}$	Deglitch time exiting OVP	V_{IN}: 11 V → 5V		450		us
V_{IN-DPM}	Low input voltage protection Restricts Iout at V_{IN-DPM}	Limit input source current to 50 mA; V_{OUT} = 3.5 V; R_{ISET} = 1.35kΩ	4.15	4.30	4.45	V
ISET SHORT CIRCUIT TEST						
R_{ISET_SHORT}	Highest resistor value considered a fault (short).	R_{ISET}: 540 Ω → 250 Ω, Iout latches off; Cycle power to reset		420	450	Ω
T_{DGL_SHORT}	Deglitch time transition from ISET short to Iout disable	Clear fault by disconnecting IN or cycling (high /low) TS/BAT_EN		1.8		ms
I_{OUT_CL}	Maximum OUT current limit regulation (Clamp)	V_{IN} = 5 V; V_{OUT} = 3.6 V; R_{ISET}: 540 Ω → 250 Ω; I_{OUT} latches off after $t_{DGL-SHORT}$	550	650	750	mA

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BATTERY SHORT PEOTECTION						
$V_{OUT(SC)}$	OUT pin short-circuit detection threshold/ pre-charge threshold	V_{OUT}:3 V → 0.5 V; No deglitch	0.75	0.8	0.85	V
$I_{OUT(SC)}$	Source current to OUT pin during short-circuit detection		7	11	15	mA
QUIESCENT CURRENT						
$I_{OUT(PDWN)}$	Battery current into OUT pin (1)	V_{IN} = 0 V; V_{OUT}=4V			75	nA
		V_{IN} = 0 V; V_{OUT}=4V 0°C to 85°C			100	nA
$I_{OUT(DONE)}$	OUT pin current, charging terminated	V_{IN} = 5 V; V_{OUT}>$V_{OUT(REG)}$		10	15	µA
$I_{IN(STDBY)}$	Standby current into IN pin	TS = GND; V_{IN} ≤5.5 V		110	145	µA
I_{CC}	Active supply current, IN pin	TS = open, V_{IN} = 5 V; TTDM – no load on OUT pin; V_{OUT}> $V_{OUT(REG)}$; IC enabled		0.5	0.8	mA
BATTERY CHARGER						
$V_{OUT(REG)}$	Output voltage	V_{IN} = 5.0 V; R_{ISET} = 1.35kΩ; $V_{TS-45°C}$≤V_{TS} ≤ $V_{TS-0°C}$	4.16	4.2	4.24	V
V_{O_HT} (REG)	Battery hot regulation voltage	V_{IN} = 5.0 V; R_{ISET} = 1.35kΩ; $V_{TS-60°C}$≤ V_{TS}≤ $V_{TS-45°C}$	4.0	4.06	4.12	V
I_{OUT} (RANGE)	Programmed output “fast charge” current range	$V_{OUT(REG)}$> V_{OUT}> V_{LOWV}; V_{IN} = 5 V; R_{ISET} = 0.54 kΩ to 13.5 kΩ	10		250	mA
V_{DO} (IN-OUT)	Drop-Out, V_{IN} – V_{OUT}	Adjust V_{IN} down until I_{OUT} = 0.2 A drop; V_{OUT} = 4.15 V; R_{ISET} = 680 Ω;			400	mV
I_{OUT}	Output “fast charge” formula	$V_{OUT(REG)}$> V_{OUT}> V_{LOWV}; V_{IN} = 5 V	K_{ISET}/R_{ISET}			A
K_{ISET}	Fast charge current factor	R_{ISET} = K_{ISET} /I_{OUT}; 20 < I_{OUT}< 250 mA	129	135	145	AΩ
		R_{ISET} = K_{ISET} /I_{OUT}; 5 < I_{OUT}< 20 mA	125	135	145	AΩ
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
%PREC	Pre-charge current, default	V_{OUT}< V_{LOWV};	18	20	22	%

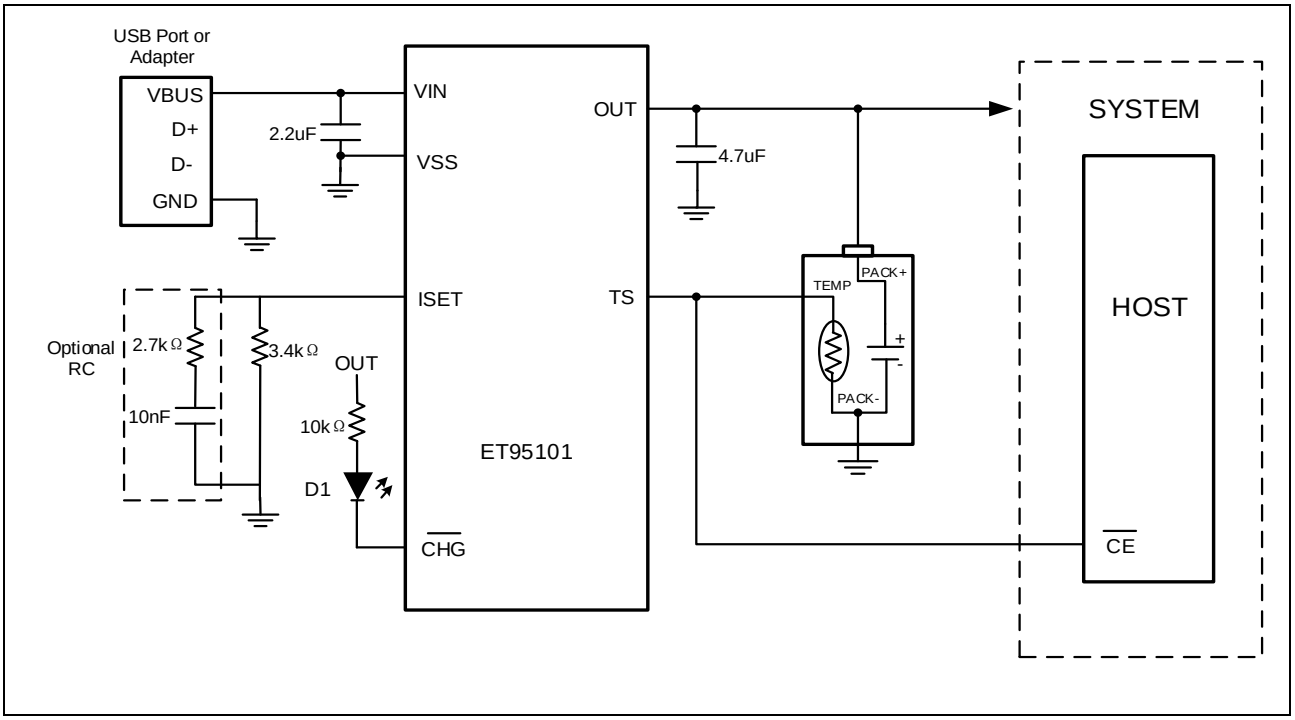
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HG	setting	R_{ISET} = 1.35 kΩ;				I_{OUT-CC}
%TERM	Termination threshold current (1)	V_{OUT}> V_{RCH}; R_{ISET} = 1.35 kΩ;	7	9	11	% I_{OUT-CC}
V_{RCH}	Recharge detection threshold –normal temp	V_{IN} = 5 V; V_{TS} = 0.5 V;	$V_{O(REG)}$ -0.125	$V_{O(REG)}$ -0.095	$V_{O(REG)}$ -0.075	V
	Recharge detection threshold –hot temp	V_{IN} = 5 V; V_{TS} = 0.2 V;	$V_{O-HT(REG)}$-0.13	$V_{O-HT(REG)}$ -0.105	$V_{O-HT(REG)}$-0.8	V
$T_{DGL (TERM)}$	Deglitch time; Termination detected	V_{IN} = 5 V; V_{TS} = 0.5 V; V_{OUT}: 4 V → 4.3V to CHG change high;		58		ms
$T_{DGL(RCH)}$	Deglitch time, recharge threshold detected	V_{IN} = 5 V; V_{TS} = 0.5 V; V_{OUT}: 4.3 V →4 V $t_{DGL(RCH)}$ is time to ISET ramp		58		ms
BATTERY DETECT ROUTINE-(NOTE:In Hot mode VO(REG) becomes VO_HT(REG))						
V_{REG-BD}	V_{OUT} reduced regulation during battery detect	V_{IN} = 5 V; V_{TS} = 0.5 V, Battery absent	$V_{O(REG)}$ -0.45	$V_{O(REG)}$ -0.4	$V_{O(REG)}$ -0.35	V
$I_{BD-SINK}$	Sink current during V_{REG-BD}	V_{IN} = 5 V; V_{TS} = 0.5V, Battery absent		2.5		mA
$T_{DGL(HI/LOW REG)}$	Regulation time at VREG or V_{REG-BD}	V_{IN} = 5 V; V_{TS} = 0.5 V, Battery absent		29		ms
T_{PRECHG}	Pre-charge safety timer value (1)	Restarts when entering pre-charge; Always enabled when in pre-charge.		1800		s
T_{MAXCH}	Charge safety timer value (1)	Clears fault or resets at UVLO, TS disable, Always enabled when in fast-charge.		36000		s
BATTERY-PACK NTC MONITOR; TS pin: 10k NTC						
$I_{NTC-10k}$	NTC bias current	V_{TS} = 0.3 V	48	50.5	53	µA
$I_{NTC-DIS-10k}$	10k NTC bias current when charging is disabled	V_{TS} = 0 V	26	30	34	µA
$I_{NTC-FLDBK-10k}$	I_{NTC} is reduced prior to entering TTDM to keep cold thermistor from entering TTDM	V_{TS}: Set to 1.525 V	4.5	6	7.5	µA
$V_{TTDM(TS)}$	Termination and timer disable mode Threshold	V_{TS}: 0.5 V → 1.7 V; Timer held in reset	1550	1600	1650	mV

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{HYS-TTDM(TS)}$	Hysteresis exiting TTDM	V_{TS}: 1.7 V → 0.5 V; Timer enabled		100		mV
$V_{CLAMP(TS)}$	TS maximum voltage clamp	V_{TS} = Open (float)	1900	2100	2300	mV
$V_{TS\_I-FLDBK}$	TS voltage where I_{NTC} is reduce to keep thermistor from entering TTDM	I_{NTC} adjustment (90 to 10%; 45 to 6.6 uA) takes place near this spec threshold; V_{TS}: 1.425 V → 1.525 V		1475		mV
$V_{TS-0°C}$	Low temperature CHG pending	Low temp charging to pending; V_{TS}: 1 V → 1.5 V	1200	1255	1310	mV
$V_{HYS-0°C}$	Hysteresis	At 0°C; Charge pending to low temp charging; V_{TS}: 1.5 V → 1 V		100		mV
$V_{TS-10°C}$	Low temperature, half charge	Normal charging to low temp charging; V_{TS}: 0.5 V → 1 V	770	800	830	mV
$V_{HYS-10°C}$	Hysteresis	At 10°C; Low temp charging to normal CHG; V_{TS}: 1 V → 0.5 V		55		mV
$V_{TS-45°C}$	High temperature	At 45°C; Normal charging to high temp CHG; V_{TS}: 0.5 V → 0.2 V	250	268	285	mV
$V_{HYS-45°C}$	Hysteresis	At 45°C; High temp charging to normal CHG; V_{TS}: 0.2 V → 0.5 V		20		mV
$V_{TS-60°C}$	High temperature disable	High temp charge to pending; V_{TS}: 0.2 V → 0.1 V	155	170	185	mV
$V_{HYS-60°C}$	Hysteresis	At 60°C; Charge pending to high temp CHG; V_{TS}: 0.1 V → 0.2 V		20		mV
$V_{TS-EN-10k}$	Charge enable threshold, (10k NTC)	V_{TS}: 0 V → 0.175 V	90	100	110	mV
$V_{TS-DIS\_HYS-10k}$	HYS below VTS-EN-10k to disable (10k NTC)	V_{TS}: 0.125 V → 0 V		12		mV

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			120		°C
$T_{J(OFF)}$	Thermal shutdown temperature			150		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			30		°C
LOGIC LEVELS ON /CHG						
V_{OL}	Output low voltage	I_{SINK} = 5 mA			0.4	V
I_{LEAK}	Leakage current into IC	V_{CHG} = 5 V			1	μA

Note1: Guaranteed by design and characterization. not a FT item.

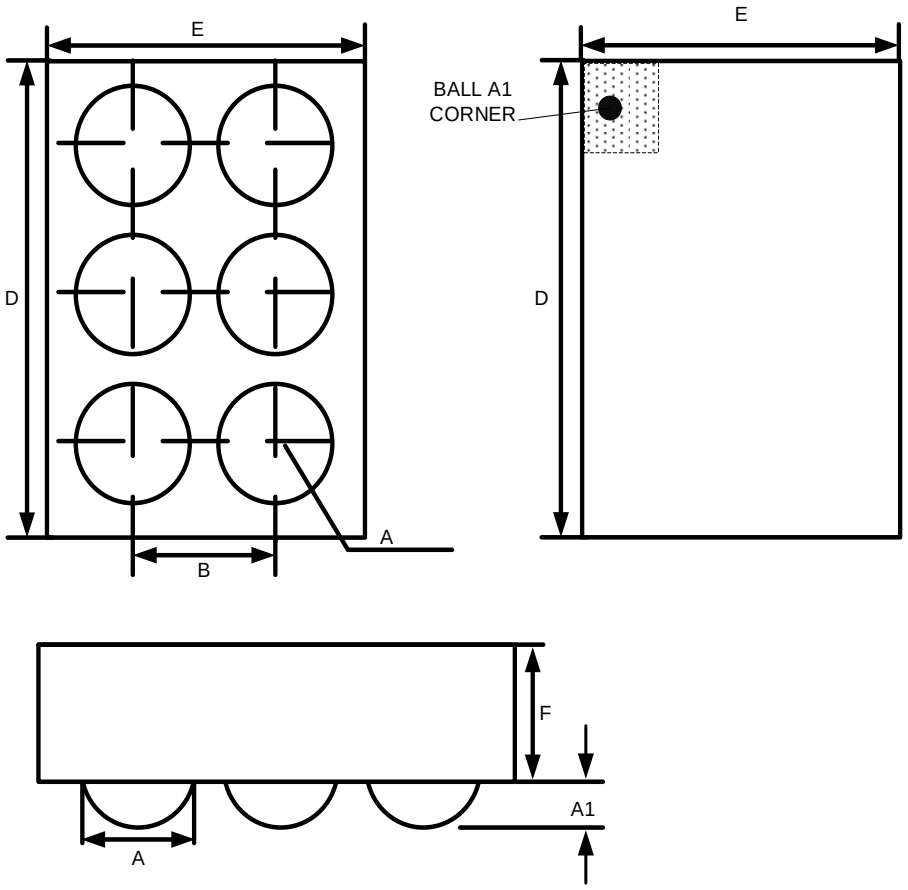
Application Circuits



Note. C_{TS}=0.22uF(ESD protection optional capacitance, connect between TS and VSS)

C_{OUT} can not less than 2.2uF.

Package Dimension



Dimensions Table (Units:mm)

Symbol	Min	Typ	Max
A	0.19	0.21	0.23
A1	0.13	0.16	0.19
B		0.4REF	
D	1.23	1.29	1.35
E	0.85	0.88	0.91
F	0.33	0.34	0.35

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	20221209	Preliminary Version	Chen Zhu Xiong	Xia Yong Jie	Liu Jia Ying
1.1	20230206	Update Typeset	Chen Zhu Xiong	Xia Yong Jie	Liu Jia Ying
1.2	20230804	Update Typeset and Spec	Yin Peng	Xia Yong Jie	Liu Jia Ying
1.3	20231115	Update EC Table Spec	Yin Peng	Xia Yong Jie	Liu Jia Ying