

10MHz, RRIO, CMOS Operational Amplifier for Cost-Sensitive Systems

General Description

ETQ85602 is a dual low-voltage (1.8 V to 5.5 V) operational amplifier (op amp) with rail-to-rail input- and output- swing capabilities. The device is highly cost-effective solutions for applications where low-voltage operation, a small footprint, and high capacitive load drive are required. Although the capacitive load drive of the ET85602 is 100 pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler. The op amp is designed specifically for low-voltage operation (1.8 V to 5.5 V).

ETQ85602 is specified for the extended industrial/automotive temperature range (-40°C to +125°C). It is available in SOP8 / MSOP8 packages.

Features

- Rail-to-rail input and output
- Low input offset voltage: ± 0.3 mV
- Unity-gain bandwidth: 10 MHz
- Low broadband noise: $10 \text{ nV}/\sqrt{\text{Hz}}$
- Low input bias current: ± 5 pA
- Low quiescent current: 550 μA
- Unity-gain stable
- Internal RFI and EMI filter
- Operational supply voltage range 1.8 V to 5.5V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Automotive AEC-Q100 Grade 1 Qualified
 - Extended temperature range of -40°C to +125°C
 - ESD HBM 2.5KV PASS
 - ESD CDM 1KV PASS

Applications

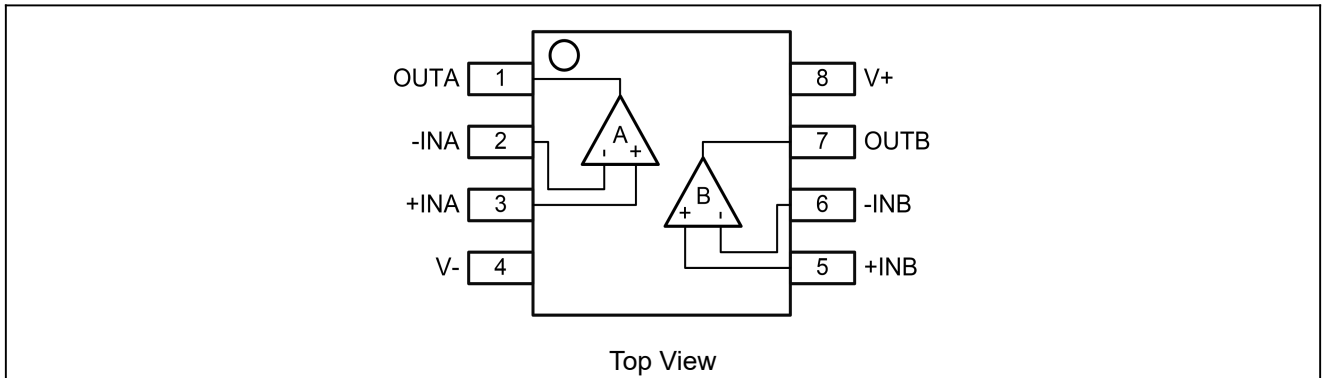
- Temperature sensors
- Smoke detectors
- Wearable devices
- Laptop computers
- Sensor signal conditioning
- Power modules
- Active filters
- Low-side current sensing

ETQ85602

Device information

Part No.	Package	MSL
ETQ85602M	SOP8	1
ETQ85602U	MSOP8	1

Pin Configuration



Pin Function

Pin Number	Symbol	Descriptions
1,7	OUT	Output
4	V-	Negative supply
3,5	+IN	Non-inverting input
2,6	-IN	Inverting input
8	V+	Positive supply

Functional Description

Operating Voltage

ETQ85602 operates from 1.8 V to 5.5 V, is unity-gain stable, and is designed for a wide range of general-purpose applications.

Rail-to-Rail Input

The input common-mode voltage range extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage.

Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the ETQ85602 delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 k Ω , the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

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Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Symbol	Parameter	Value	Unit
V _S	Supply Voltage:(V+) - (V-)	0 to 6	V
V _{IC}	Common-mode Input Voltage ⁽¹⁾	(V-)-0.5 to (V+)+0.5	V
V _{ID}	Differential Input Voltage ⁽¹⁾	(V+) - (V-)+0.2	V
I _{IN}	Signal input terminals Current ⁽¹⁾	-10 to +10	mA
I _{SC}	Output short-circuit current ⁽²⁾	Continuous	
V _{ESD}	ESD (Human Body Model) ⁽³⁾	±2500	V
	ESD (Component Discharge Model) ⁽⁴⁾	±1000	V
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _{J(MAX)}	Max Junction Temperature Range	+150	°C

Note1: Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.

Note2: Short-circuit to ground, one amplifier per package.

Note3: HBM tested per AEC-Q100-002(EIA/JESD22-A114);

Note4: CDM tested per AEC-Q100-011(EIA/JESD22-C101);

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
R _{θJA}	SOP8	Thermal Characteristics,	157.6	°C/W
	MSOP8	Thermal Resistance, Junction-to-Air	201.2	°C/W

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V _S	Supply Voltage: (V+) - (V-)	1.8(±0.9) ~ 5.5(±2.75)	V
T _A	Operating Temperature Range	-40 ~ +125	°C

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Electrical Characteristics

$V_S = (V+) - (V-) = 1.8 \text{ V to } 5.5 \text{ V}$ ($\pm 0.9 \text{ V to } \pm 2.75 \text{ V}$), $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S/2$, and $V_{CM} = V_{OUT} = V_S/2$ (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFFSET VOLTAGE						
V _{OS}	Input offset voltage	V _S = 5 V		±0.3	±2.5	mV
		V _S = 5 V, T _A = -40°C to 125°C			±3.5	
ΔV _{OS} /ΔT	Input offset voltage vs temperature	V _S = 5 V, T _A = -40°C to 125°C		±0.53		μV/°C
PSRR	Input offset voltage vs power supply	V _S = 1.8 to 5.5 V, V _{CM} = (V-)		±7	±80	μV/V
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range	V _S = 1.8 V to 5.5 V	(V-)-0.1		(V+)+0.1	V
CMRR	Common-mode rejection ratio	V _S = 5.5 V, (V-) - 0.1 V < V _{CM} < (V+) - 1.4 V, T _A = -40°C to 125°C	70	103		dB
		V _S = 5.5 V, V _{CM} = -0.1 V to 5.6 V, T _A = -40°C to 125°C	57	75		
		V _S = 1.8 V, (V-) – 0.1 V < V _{CM} < (V+) – 1.4 V, T _A = -40°C to 125°C		88		
		V _S = 1.8 V, V _{CM} = -0.1 V to 1.9 V, T _A = -40°C to 125°C		70		
INPUT BIAS CURRENT						
I _B	Input bias current	V _S = 5 V		±5		pA
I _{OS}	Input offset current			±5		pA
NOISE						
E _n	Input voltage noise (peak to peak)	f = 0.1 Hz to 10 Hz, V _S = 5 V		4.77		μV _{PP}
e _n	Input voltage noise density	f = 1 kHz, V _S = 5 V		16		nV/√Hz
		f = 10 kHz, V _S = 5 V		10		
i _n	Input current noise density ⁽⁵⁾	f = 1 kHz, V _S = 5 V		23		fA/√Hz
INPUT CAPACITANCE						
C _{ID}	Differential ⁽⁵⁾			2		pF
C _{IC}	Common-mode ⁽⁵⁾			4		pF

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Electrical Characteristics (Continued)

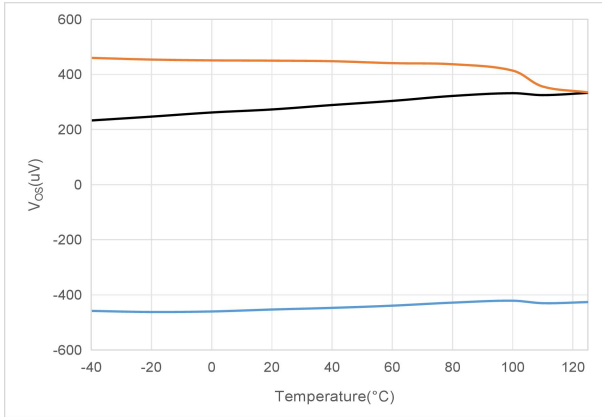
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OPEN-LOOP GAIN						
A _{OL}	Open-loop voltage gain	V _S = 1.8 V, R _L = 10 kΩ (V-) + 0.04 V < V _O < (V+) - 0.04 V		100		dB
		V _S = 5.5 V, R _L = 10 kΩ (V-) + 0.1 V < V _O < (V+) - 0.1 V	104	130		
		V _S = 1.8 V, R _L = 2 kΩ (V-) + 0.06 V < V _O < (V+) - 0.06 V		100		
		V _S = 5.5 V, R _L = 2 kΩ (V-) + 0.15 V < V _O < (V+) – 0.15 V		130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V _S = 5 V, G = +1		10		MHz
φ _m	Phase margin	V _S = 5 V, G = +1		55		°
SR	Slew rate	V _S = 5 V, G = +1		6		V/μs
t _s	Settling time ⁽⁵⁾	To 0.1%, V _S = 5 V, 2V step, G = +1, C _L = 100 pF		0.5		μs
		To 0.01%, V _S = 5 V, 2V step, G = +1, C _L = 100 pF		1		
t _{OR}	Overload recovery time	V _S = 5 V, V _{IN} × gain > V _S		0.2		μs
THD+N	Total harmonic distortion + noise	V _S = 5.5 V, V _{CM} = 2.5 V, V _O = 1 V _{RMS} , G = +1, f = 1 kHz,		0.0008		%
OUTPUT						
V _O	Voltage output swing from supply rails	V _S = 5.5 V, R _L = 10 kΩ			20	mV
		V _S = 5.5 V, R _L = 2 kΩ			60	
I _{SC}	Short-circuit current	V _S = 5 V		±50		mA
Z _O	Open-loop output impedance ⁽⁵⁾	V _S = 5 V, f = 10MHz		100		Ω
POWER SUPPLY						
V _S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I _Q	Quiescent current per amplifier	I _O = 0 mA, V _S = 5.5 V		550	800	μA
		I _O = 0 mA, V _S = 5.5 V, T _A = -40°C to 125°C			850	

Note5: Guaranteed by design.

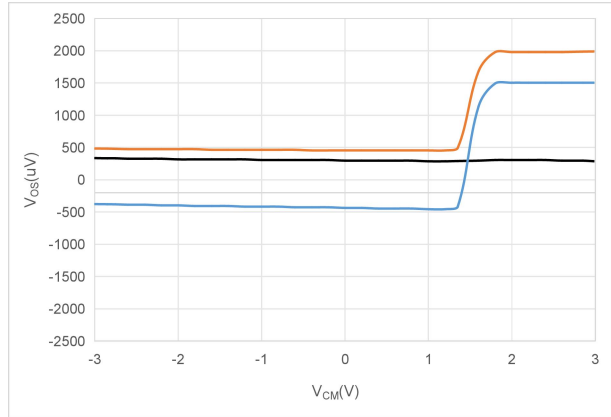
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Typical Characteristics

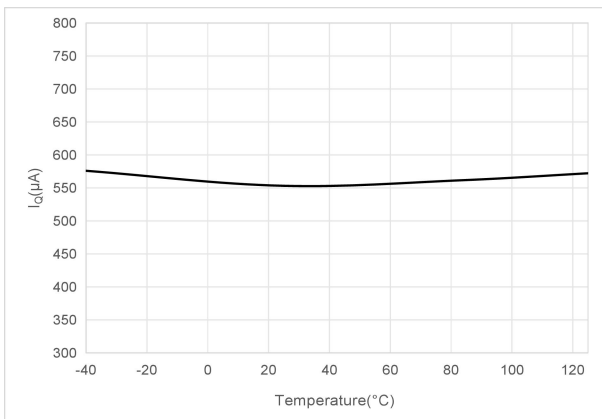
$V_S = 5.5\text{ V}(\pm 2.75\text{ V})$, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



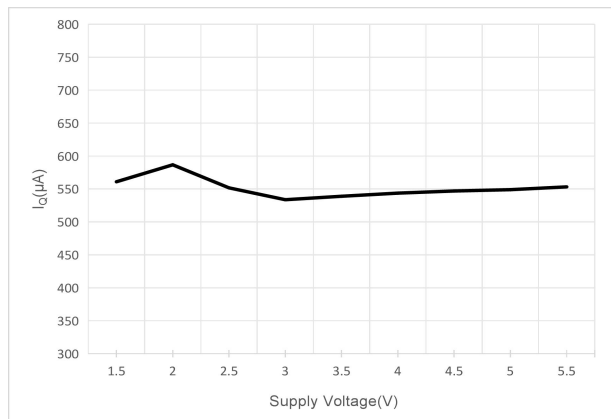
Offset Voltage vs Temperature



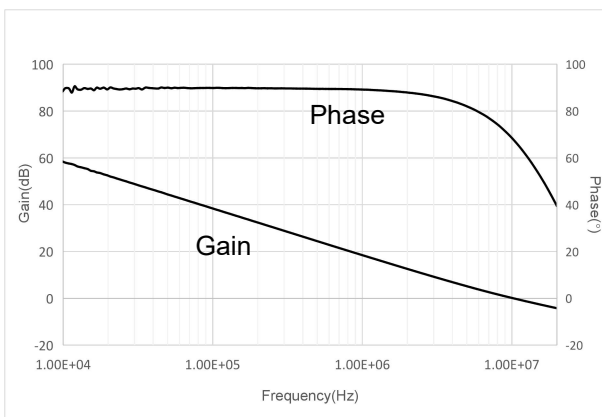
Offset Voltage vs Common-Mode Voltage



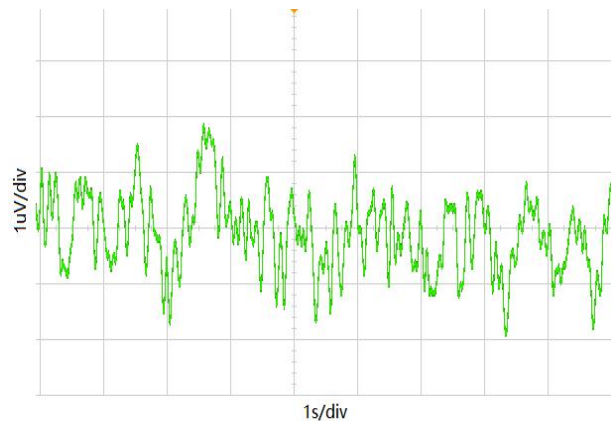
Quiescent Current vs Temperature



Quiescent Current vs Supply Voltage



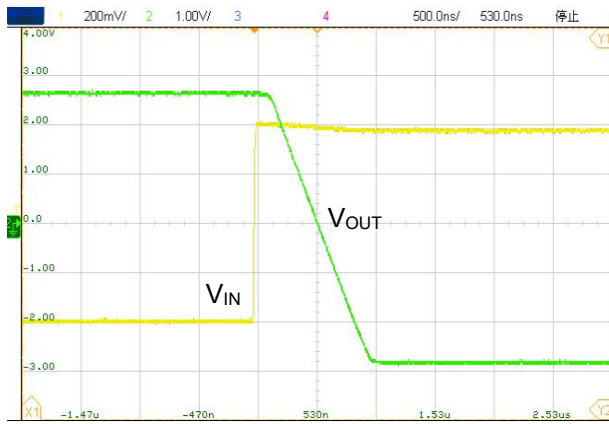
Open-Loop Gain vs Frequency



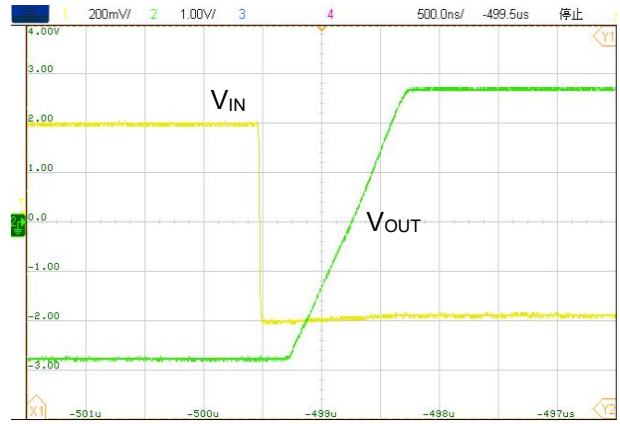
0.1 Hz to 10 Hz Noise

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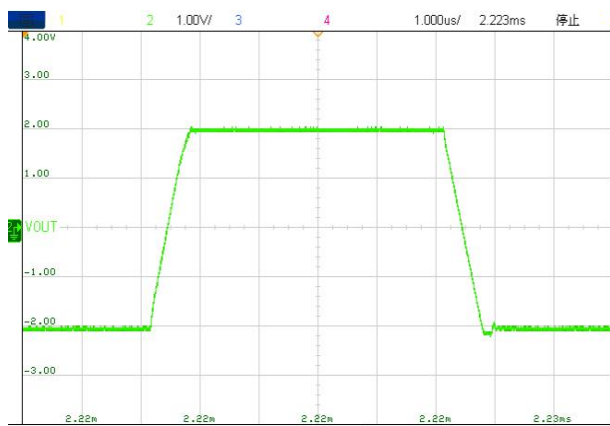
Typical Characteristics (Continued)



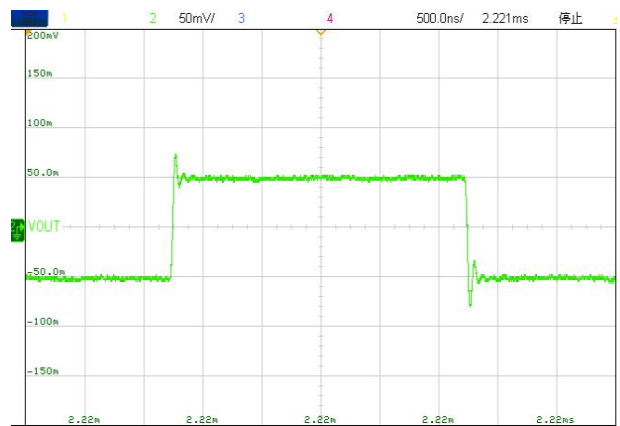
Positive Overload Recovery
($G = -10$)



Negative Overload Recovery
($G = -10$)



Large-Signal Step Response
($G = +1$)



Small-Signal Step Response(100 mV)
($G = +1, R_L = 10 \text{ k}\Omega, C_L = 100 \text{ pF}$)

Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.

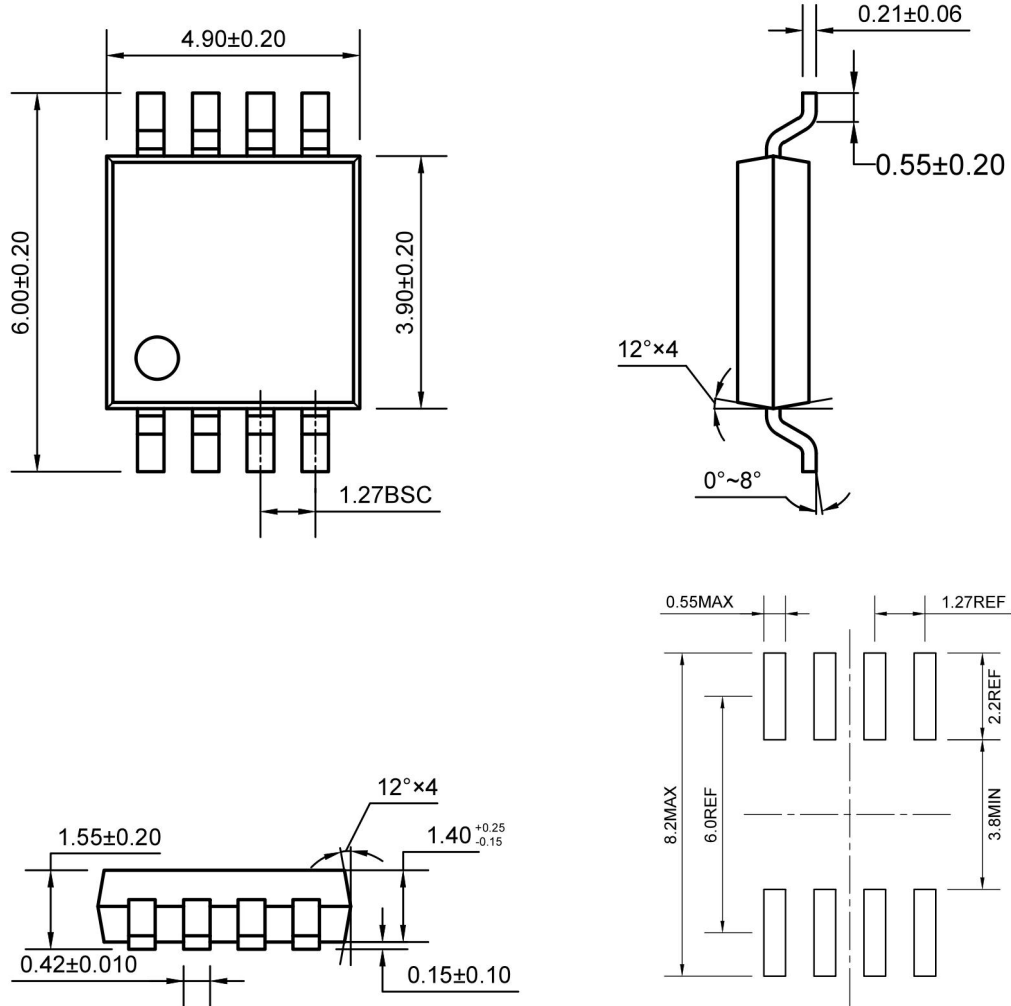
To reduce parasitic coupling, run the input traces as far away from the supply lines and digital signal as possible. Low-ESR, 0.1 μF ceramic bypass capacitors must be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single supply applications.

Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

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Package Dimension

SOP8

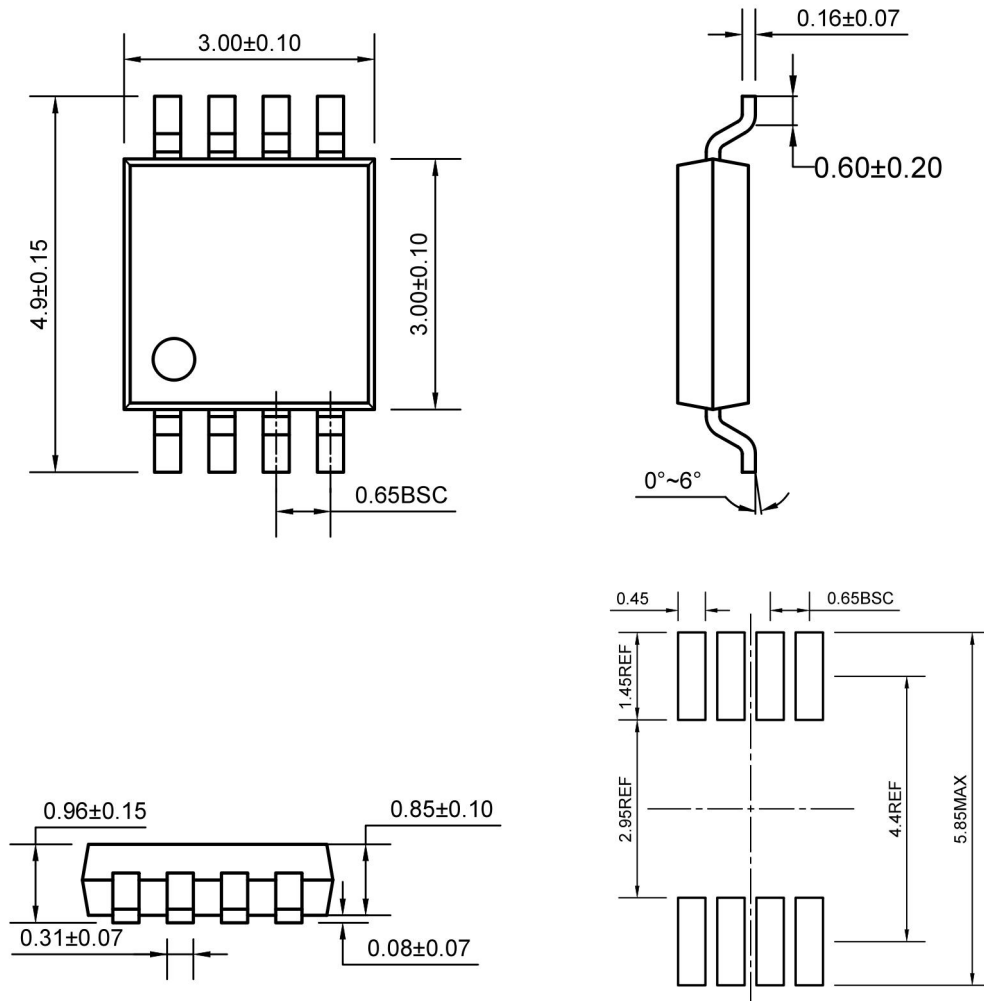


Recommended Land Pattern

Unit: mm

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MSOP8



Recommended Land Pattern

Unit: mm

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Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-04-21	Preliminary Version	Huyt	Wanggp	Liujoy
1.0	2023-08-31	Original Version	Huyt	Chenh	Liujoy
1.1	2023-9-27	Naming updates	Shibo	Wanggp	Liujoy
1.2	2023-10-19	ETQ version	Shibo	Wanggp	Liujoy
1.3	2025-03-25	Update Typical Characteristics	Huyt	Tangyx	Liujoy